Road to Chiplets: Design Integration

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Cost and Yield Analysis of Chiplet Packaging

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Agenda

- Introduction
- Process Flows
- Cost Breakdown
- Design Cost Comparison
- Yield Analysis
- Summary

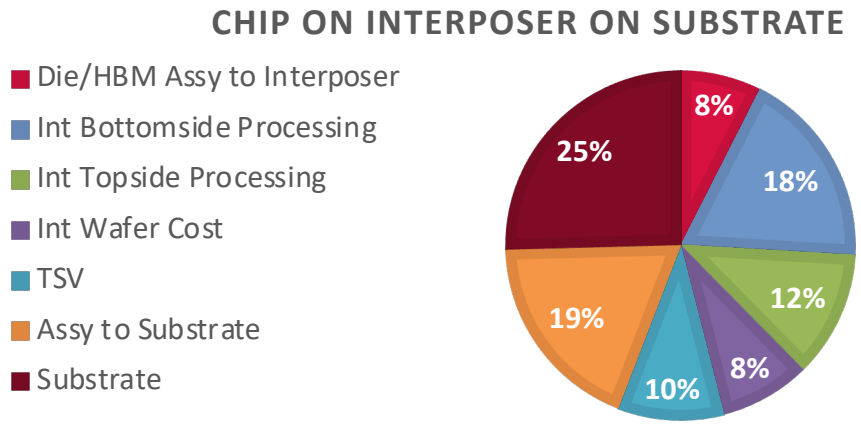
Introduction

- When building a design around chiplets, there are many factors to consider, including:
  - Industry standards (or lack thereof)
  - Availability of chiplets within the supply chain
  - Size requirements
  - Cost
- Even if all design requirements can be met by the current supply chain, the chiplet design will not be produced if the cost is too high
- Basic tradeoff between a monolithic SoC die and a series of chiplets is a **reduction** in die costs countered by an **increase** in packaging costs
  - Reduction in die costs comes from using advanced (expensive) nodes ONLY where required
  - Instead of a large monolithic die, the entirety of which must be at the node required for its most advanced function, chiplets provide the opportunity to mix and match mature and advanced nodes
  - A 10x10mm die at 10nm is about twice as much as a 10x10mm die at 28nm

Activity Based Cost Modeling

- Bottom-up approach to cost that accounts for every cost component for every activity
  - The time required to complete the activity
  - The amount of labor dedicated to the activity
  - The cost of material required to perform that activity – both consumable and permanent material
  - Any tooling cost
  - The depreciation cost of the equipment required to perform the activity
  - The yield loss associated with the activity
- Detailed output enables results to be seen in detail or rolled up in categories

Step Name	Labor Cost/Wafer	Capital Cost/Wafer	Tooling Cost/Wafer	Material Cost/Wafer	Yield Cost
RDL Spin coat	$ 0.08	$ 4.63	$ -	$ 4.38	$ 0.062
RDL Mask Cost	$ -	$ -	$ -	$ 0.21	$ 0.001
RDL Expose	$ 0.02	$ 2.07	$ -	$ -	$ 0.014
RDL Develop	$ 0.03	$ 1.54	$ -	$ 0.55	$ 0.014
RDL Cure	$ 0.08	$ 0.19	$ -	$ -	$ 0.002

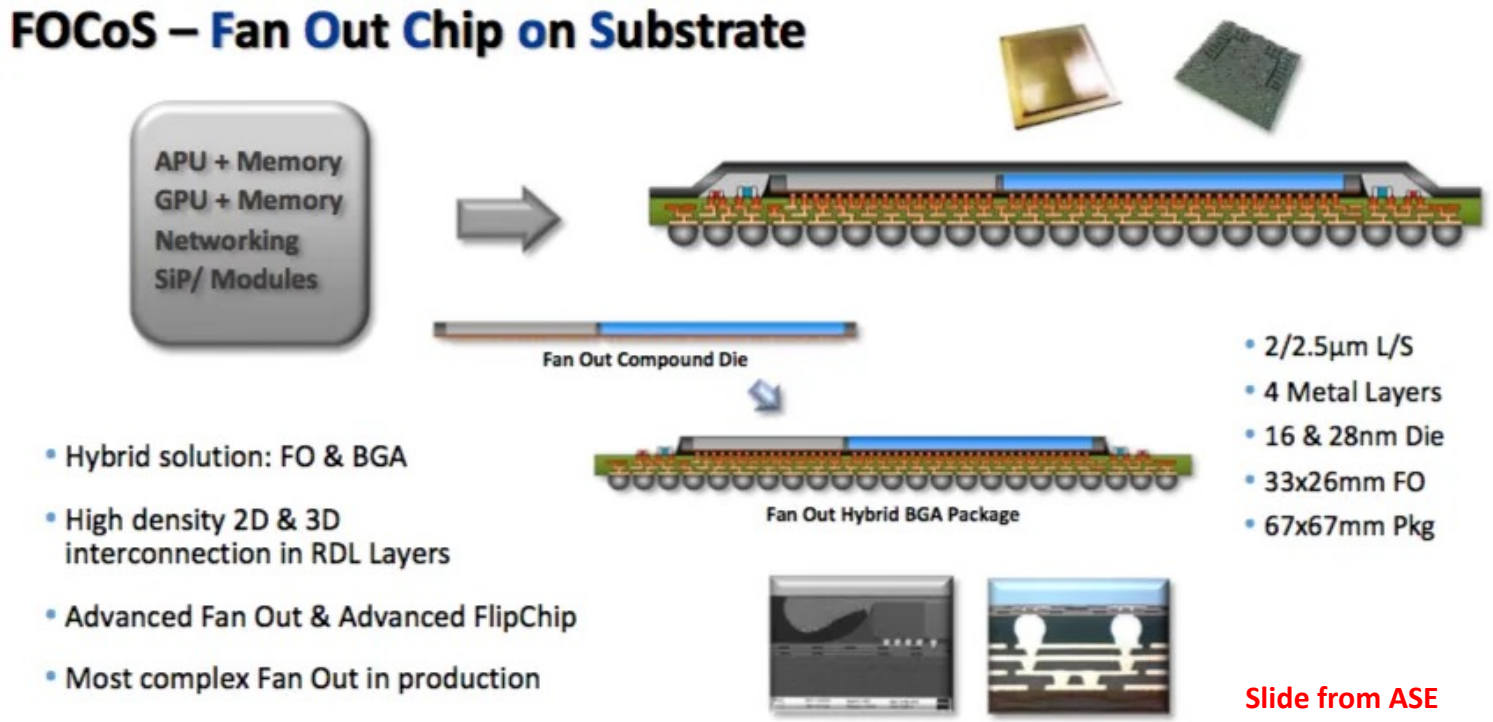


Process Flow Overviews

- Upcoming slides briefly introduce three technologies suitable for packaging chiplets
- Process flows are genericized
  - Sometimes individual activities are listed, sometimes groups of activities
  - Any process flow may have variations
- When deciding between these three (or other) process flows, it's not just about cost
  - Different advanced packaging options will support different sizes, different number of chiplets, etc.

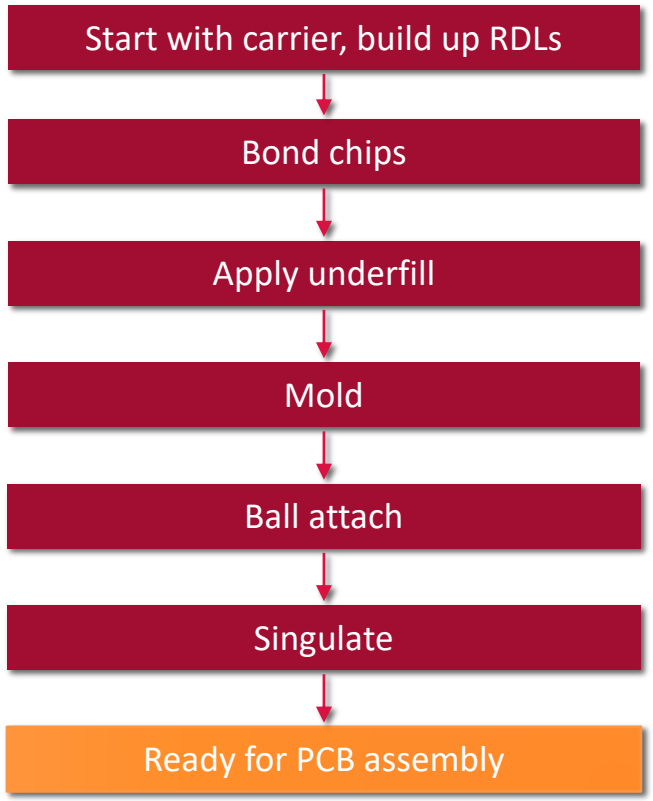
Fan-out on Substrate

- One solution to avoid an interposer
  - ASE example shown below; others (Amkor, TSMC, etc.) have similar solutions
  - Main features that differentiate this from standard fan-out → HBM support, finer line/space RDLs

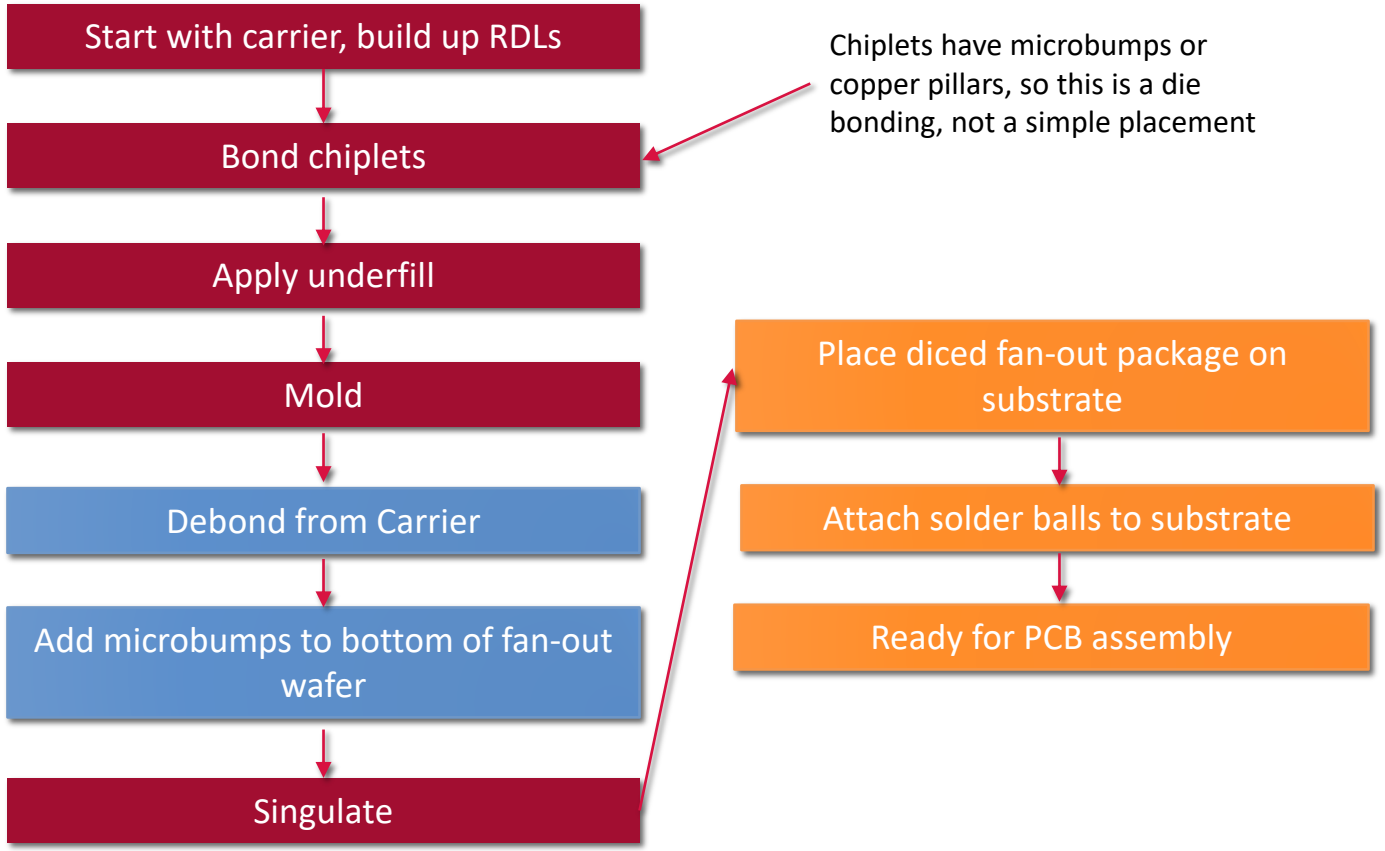


Fan-out on Substrate

Standard Chip-last Fan-out



Chip-last Fan-out on Substrate



Fan-out with Embedded Silicon Bridges

- Another solution to avoid an interposer
- Embed a piece of silicon in a fan-out module to provide interconnect paths between die
  - Requires less silicon than a full silicon interposer
  - SPIL has FOEB (Fan-out Embedded Bridge), Intel has EMIB (Embedded Multi-die Interconnect Bridge), etc.

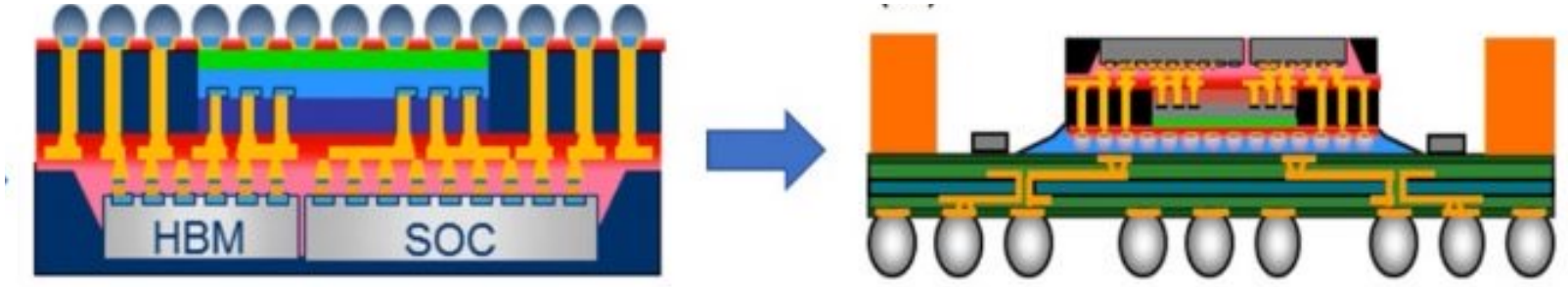
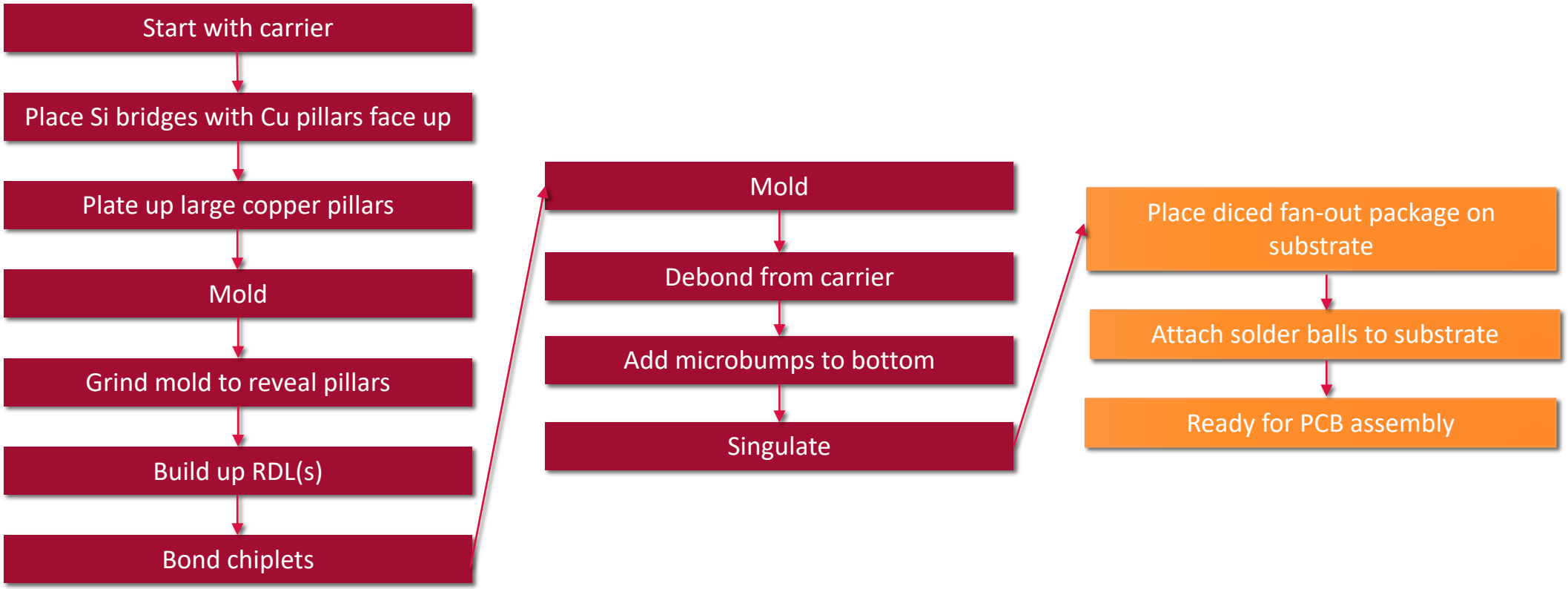


Image from SPIL

Fan-out with Embedded Silicon Bridges



2.5D Packaging with Silicon Interposer

- Chiplets are placed on a silicon wafer with interconnect built up on it
  - Interposer plus chiplets is placed on a substrate, just like in previous examples
- Chips are placed side-by-side, avoiding the need for vias in chips and directly stacking them
  - Vias are instead put in the silicon interposer

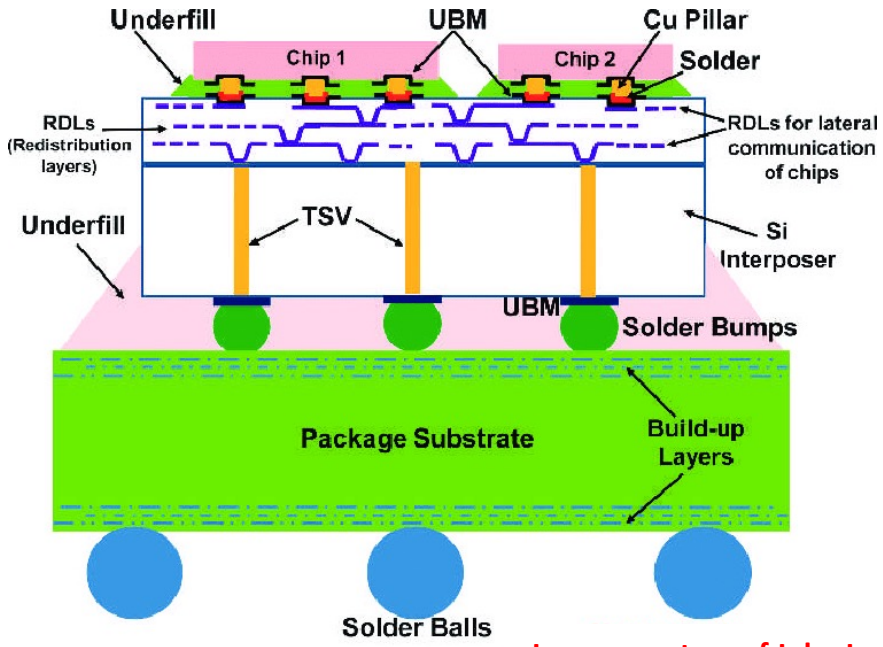
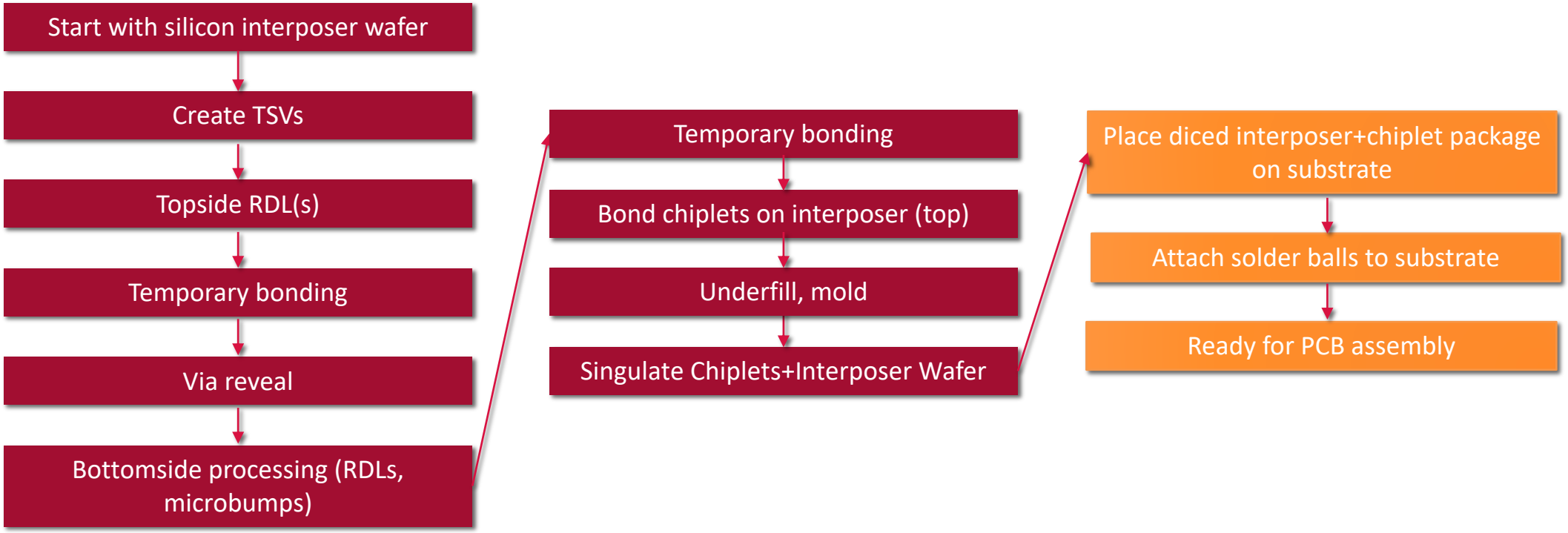


Image courtesy of John Lau

2.5D Packaging with Silicon Interposer

Chip on Interposer on Substrate

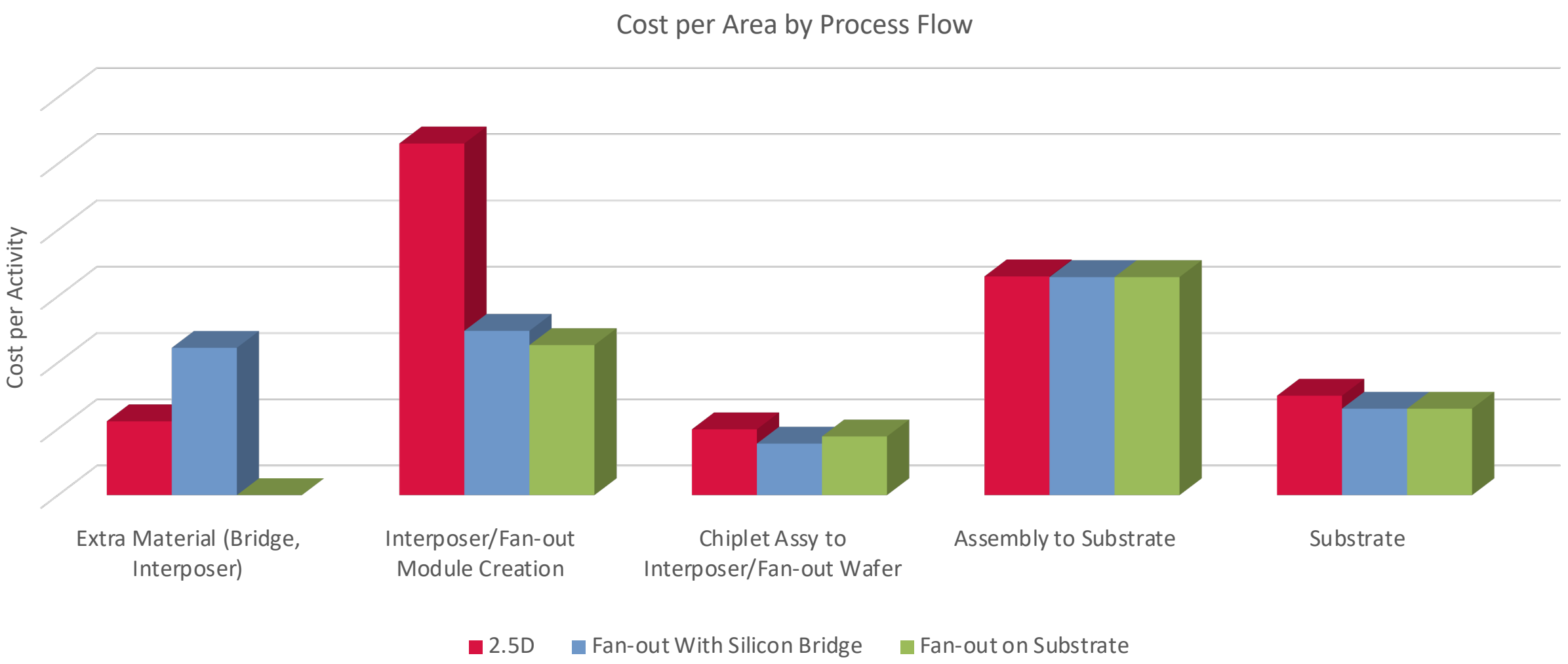


Cost Breakdown

- Three designs created for analysis
- Cost results based on area since designs aren't equivalent
  - Cost breakdown won't include incoming die cost, will include material costs specific to the process
    - Raw silicon that becomes the interposer
    - Embedded silicon pieces
  - No overhead or profit margin included
  - Factory location (impacting labor rate) same for all
  - Same substrate structure assumed for all
  - RDL count kept low to simplify

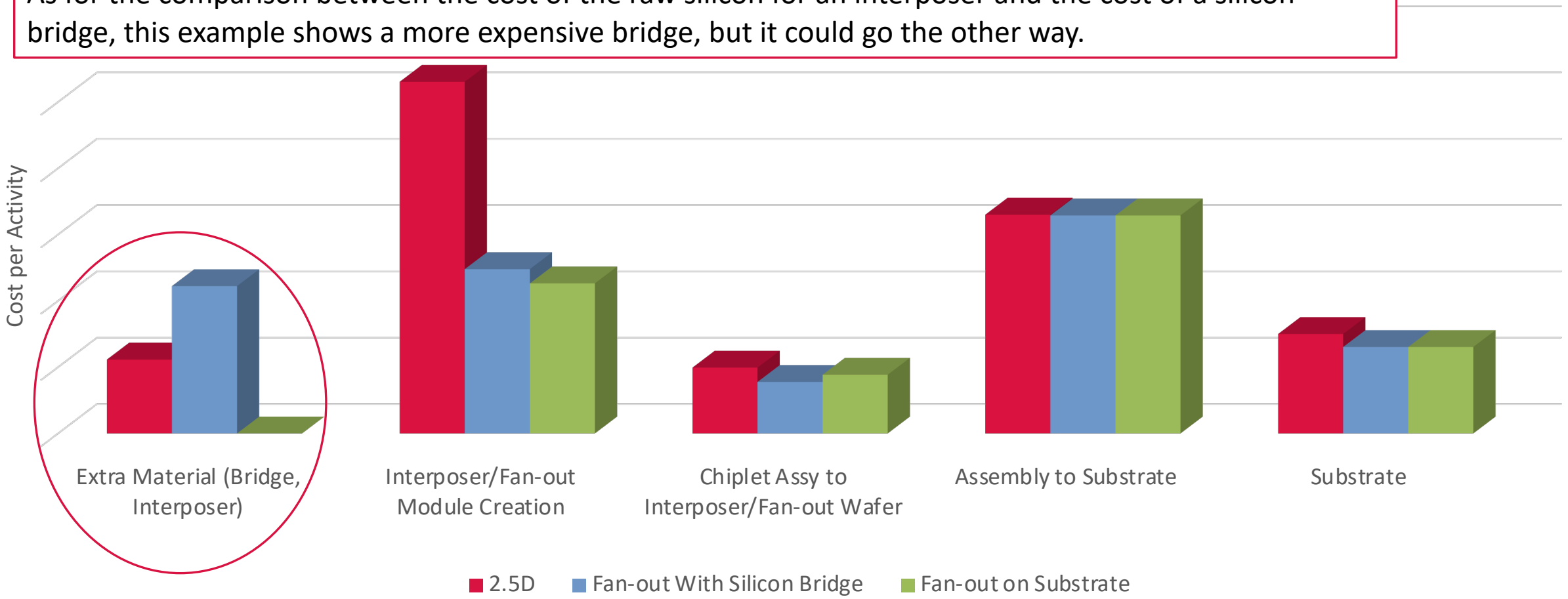
	Fan-out on Substrate	Silicon Bridge	2.5D
Interposer/Fan-out Module Size (mmxmm)	15x15	15x15	20x20
Substrate Size (mmxmm)	25x25	25x25	30x30
BOM Items	2 die	2 die, 1 Si bridge	1 die, 4 HBMs
RDLs	2	1	1 dual damascene on top, 1 OSAT-style on bottom

Cost Breakdown



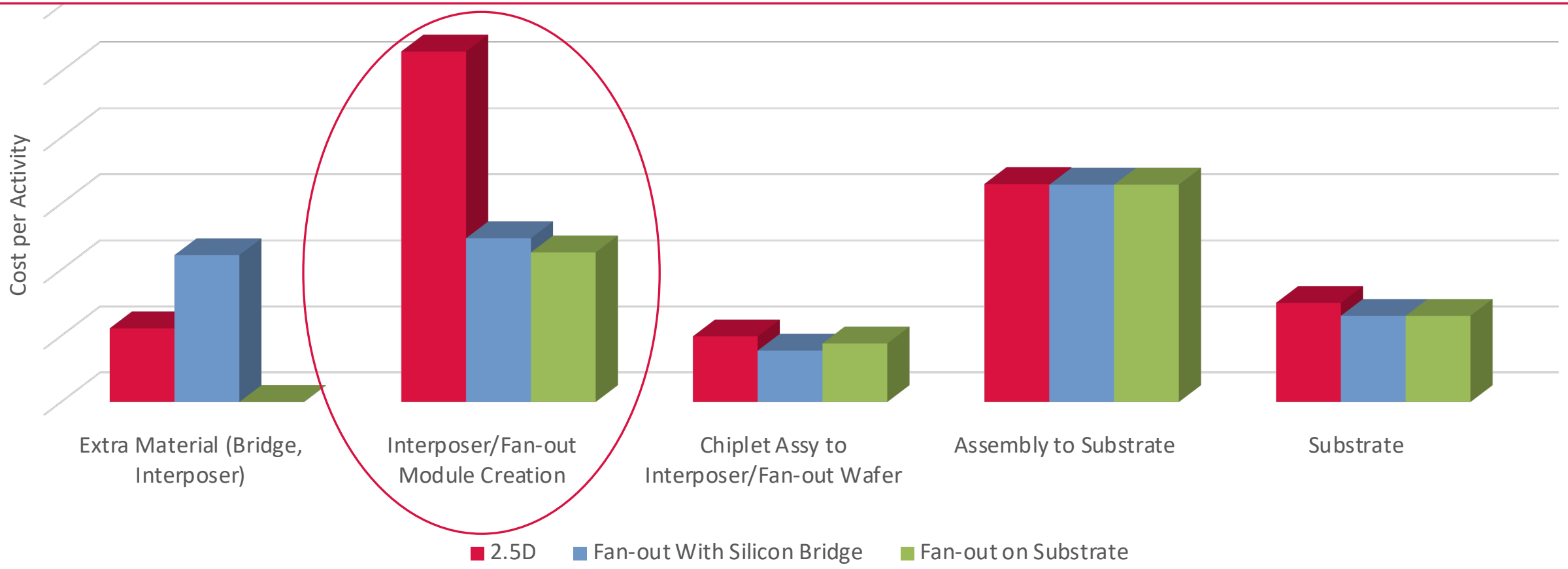
Cost Breakdown

Fan-out on substrate does not have extra silicon coming in, so that cost is zero.
As for the comparison between the cost of the raw silicon for an interposer and the cost of a silicon bridge, this example shows a more expensive bridge, but it could go the other way.



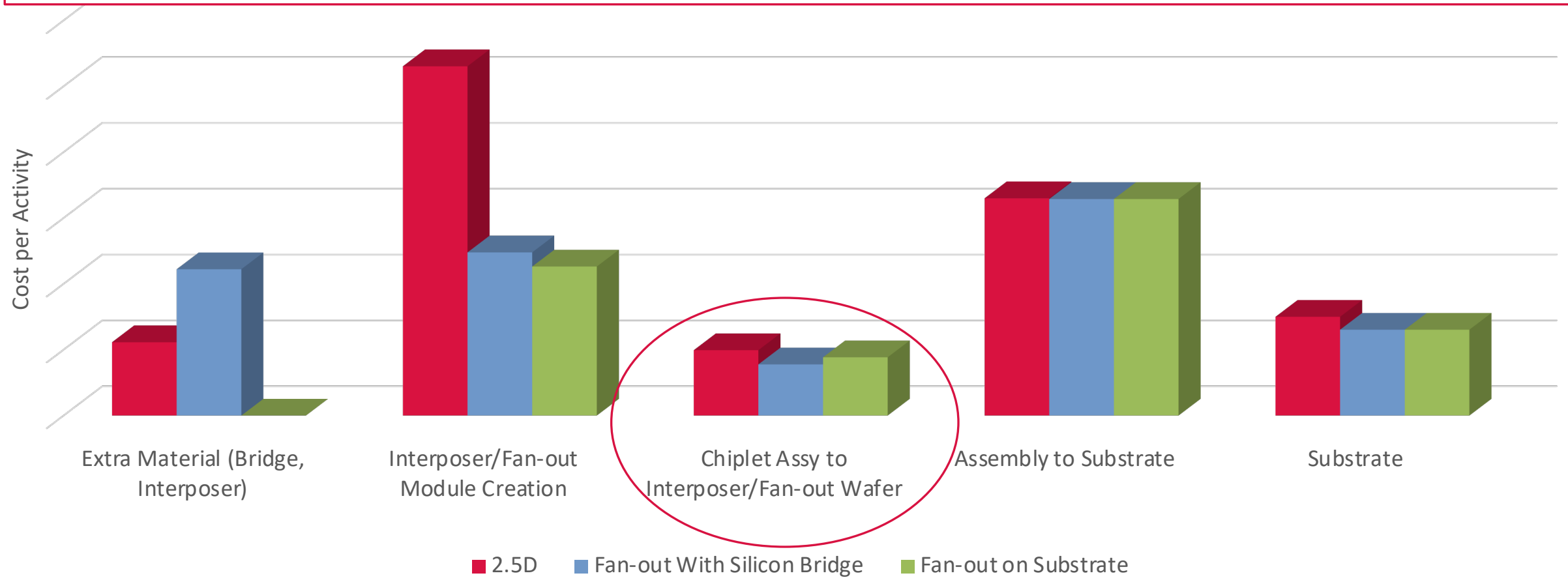
Cost Breakdown

Creating an interposer is more expensive than either fan-out module due to the addition of TSVs plus all the interconnect. The fan-out on substrate is slightly more expensive than the silicon bridge case because it has two RDLs. The silicon bridge scenario has large copper pillars, however, which almost offset the cost of the extra RDL needed for fan-out on substrate.



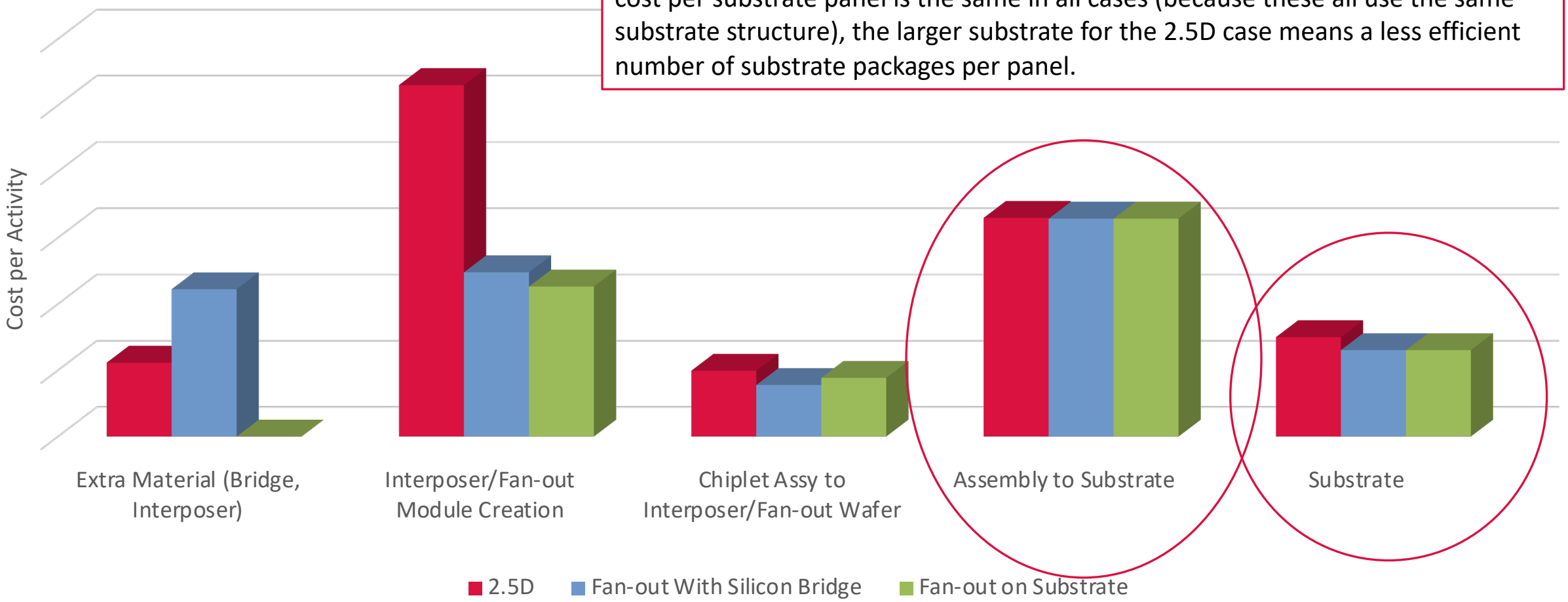
Cost Breakdown

Similar costs across technologies, as all the process flows have the same activities here: bonding of chiplets, underfill, mold, and debonding.

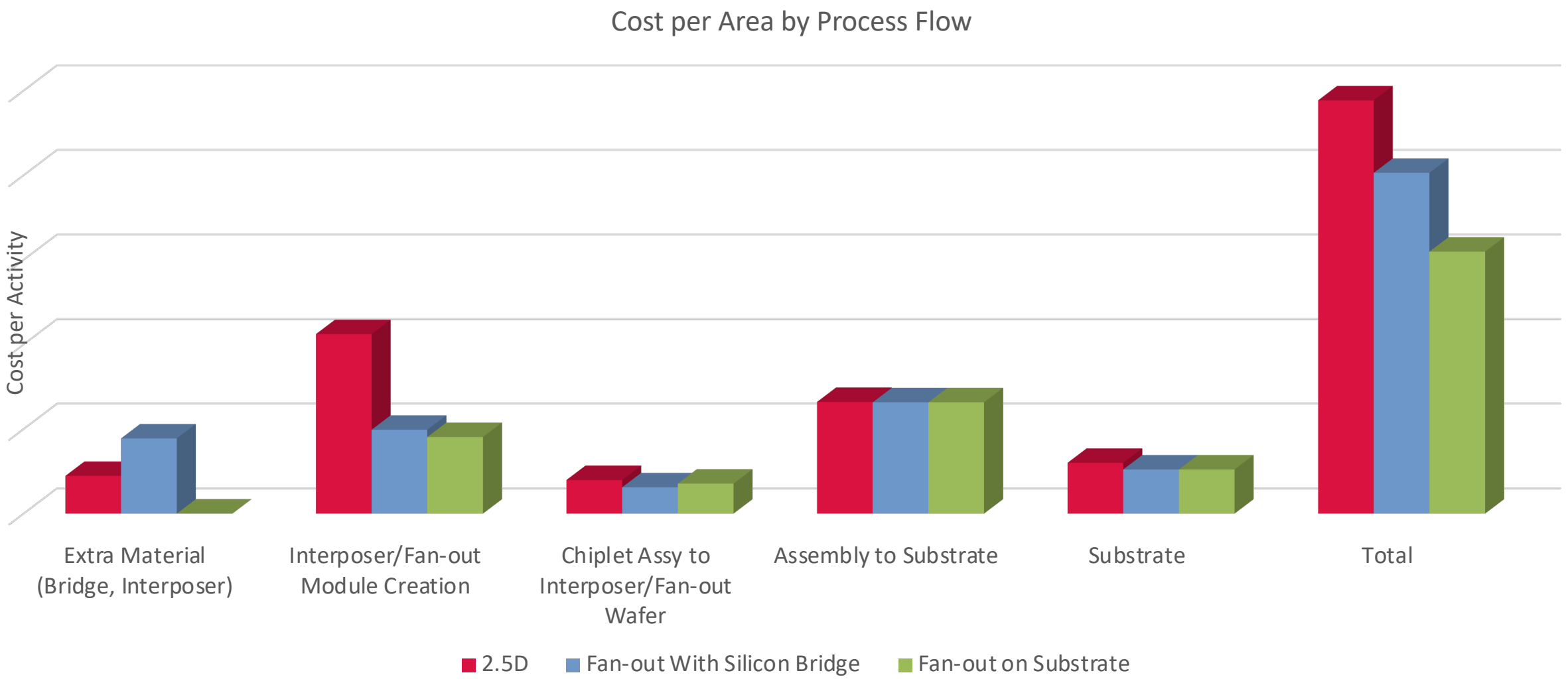


Cost Breakdown

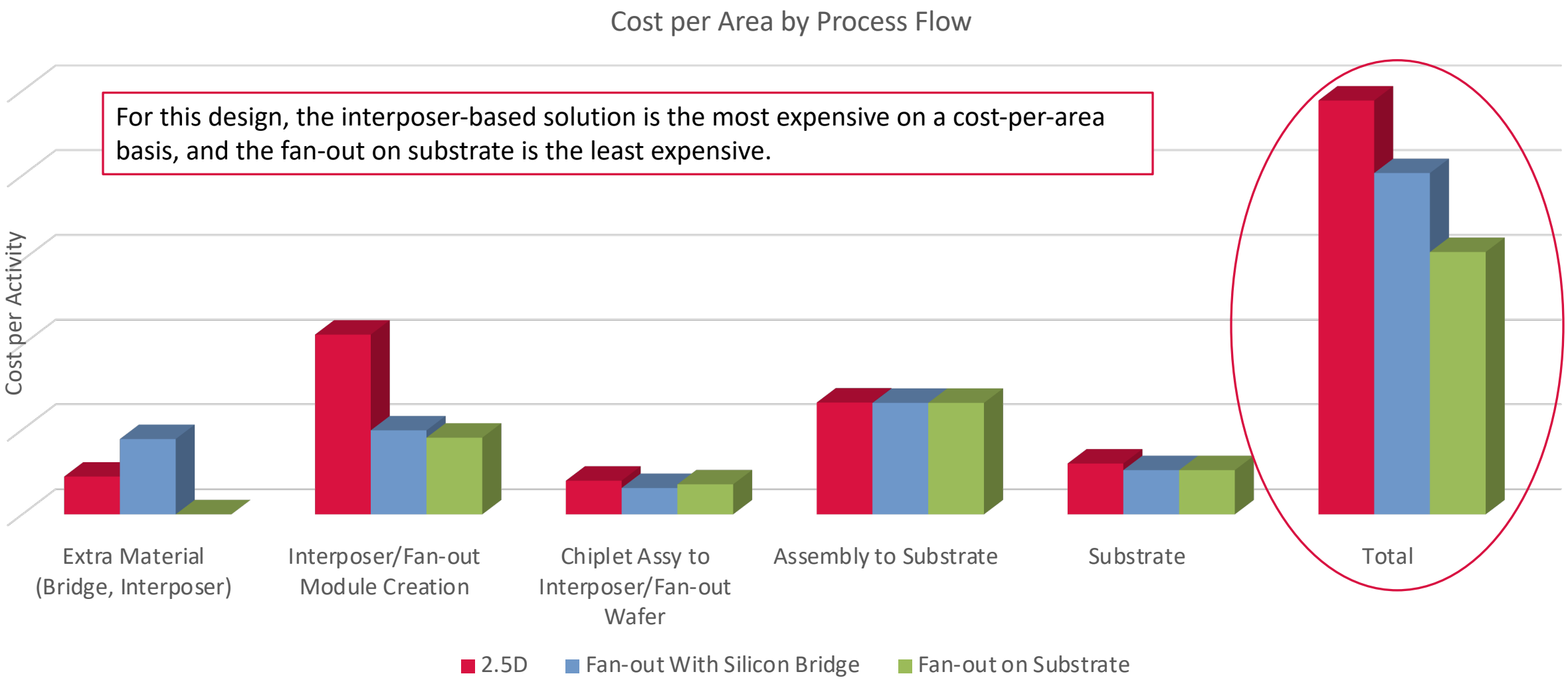
The substrate is slightly more expensive per area in the 2.5D case. Although the cost per substrate panel is the same in all cases (because these all use the same substrate structure), the larger substrate for the 2.5D case means a less efficient number of substrate packages per panel.



Cost Breakdown



Cost Breakdown



Design Comparison

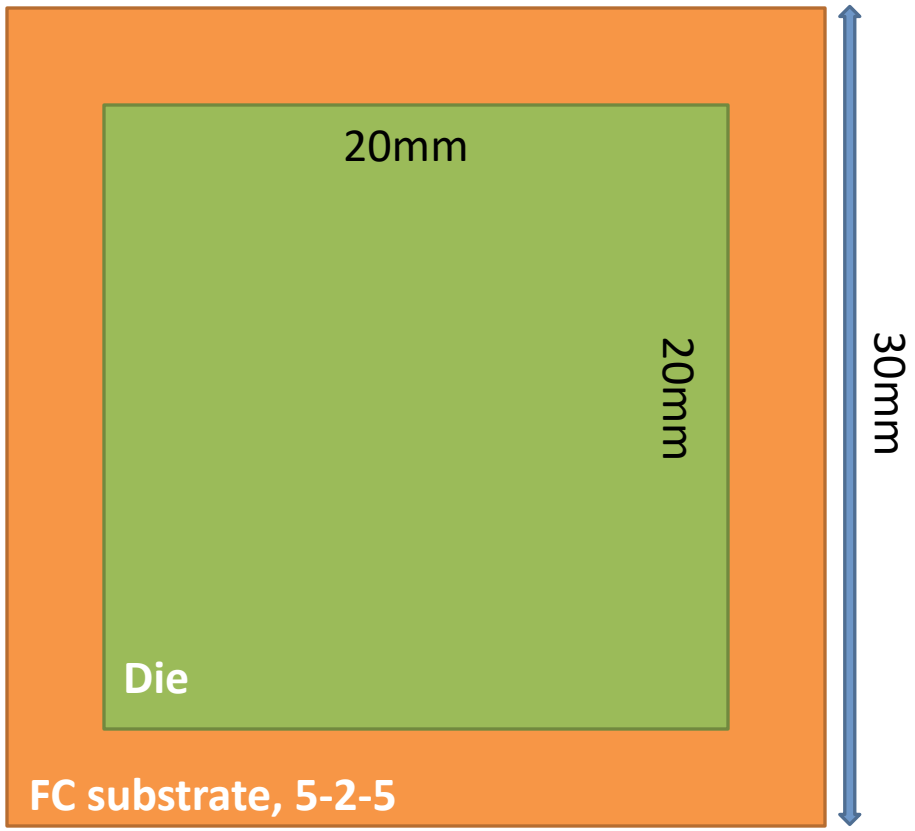
- Reminder: Basic tradeoff between a monolithic die and a series of chiplets is a **reduction** in die costs countered by an **increase** in packaging costs
- Design factors make this basic tradeoff complicated
  - Die area → Total die area might increase with chiplets
  - Substrate structure and size
    - How much larger of a substrate is needed for the advanced packaging scenarios?
    - Does the substrate need an additional layer? Can a layer be removed?
  - Number of RDLs
    - How many RDLs are needed in the various advanced packaging scenarios?

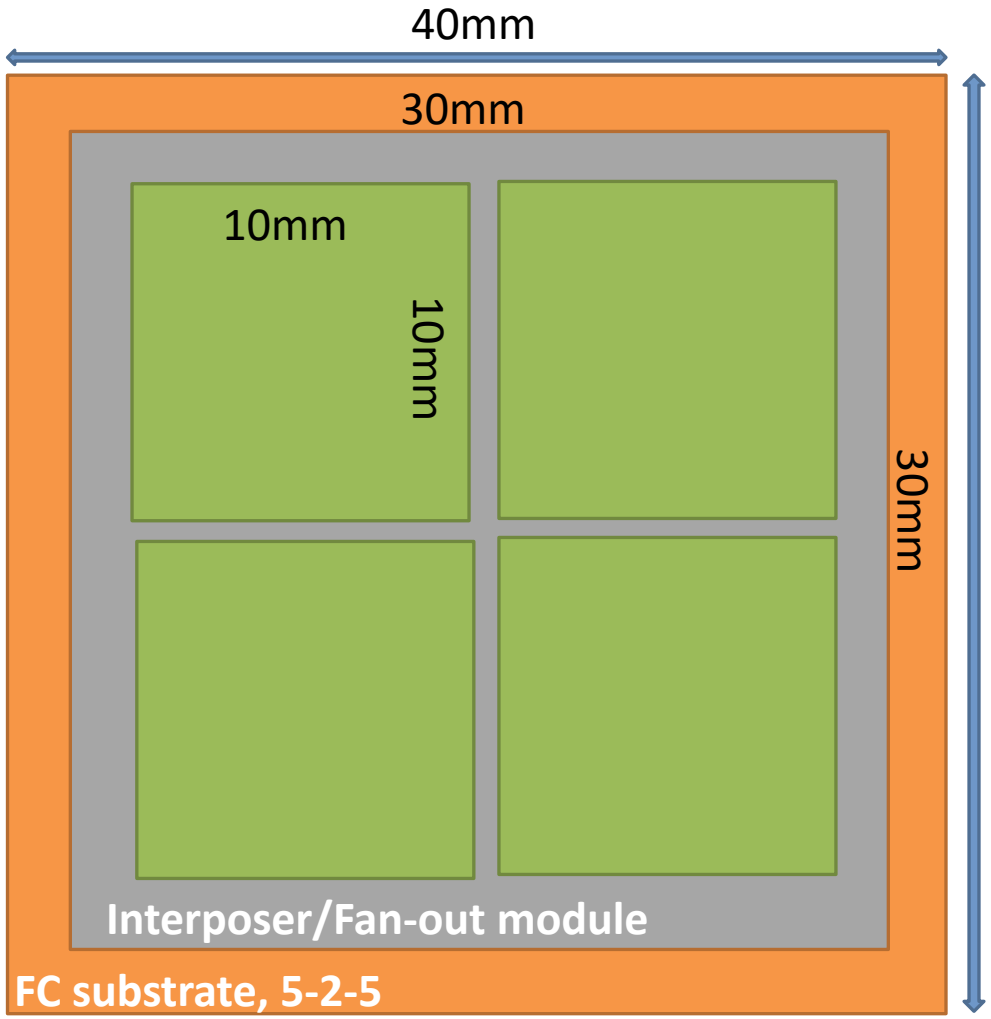
Design Comparison: 10nm

- Compare monolithic die to 4 chiplets
  - 10nm monolithic die
  - 10nm chiplet, 45nm chiplet, two 28nm chiplets
  - Node pricing based on published data about the cost of wafers at different nodes
- Keep die area the same between designs
  - One 20x20mm die versus four 10x10mm chiplets
- Assume larger substrate needed in chiplet scenario
  - To support the interposer or fan-out module

Design Comparison: 10nm

Monolithic die, flip chip connection





4 chiplets on interposer or fan-out module, larger substrate required, same build up

Initial Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.93
Total	**1.00**	**1.04**	**0.93**	**1.04**

All cost categories shown relative to the Monolithic Die scenario, except Interposer/Fan-out module, which is shown relative to the Silicon Interposer case

- With these assumptions, the fan-out on substrate package is the only option that is more cost-effective than the monolithic die

Initial Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.93
Total	**1.00**	**1.04**	**0.93**	**1.04**

All cost categories shown relative to the Monolithic Die scenario, except Interposer/Fan-out module, which is shown relative to the Silicon Interposer case

- Substrate
  - Due to the size increase from 30x30mm to 40x40mm, this cost is higher in the advanced packaging scenarios
- Die
  - Raw cost of the die based on the per area cost of silicon at each node
  - Chiplets (10nm, 45nm, 28nm x2, all 10x10mm) are about 60% of the cost of a single 10nm die (20x20mm)
  - Cost of silicon bridges is included here, causing this category to be slightly more expensive for embedded silicon bridges than for the other two advanced packaging scenarios

Initial Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
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Total	**1.00**	**1.04**	**0.93**	**1.04**

All cost categories shown relative to the Monolithic Die scenario, except Interposer/Fan-out module, which is shown relative to the Silicon Interposer case

- Die Prep
  - Cost to bump and dice the incoming chiplets is almost the same as the cost to bump and dice the large die
  - This category is not a cost driver and doesn't represent a substantial cost for any of these designs
- Assembly to substrate
  - Assembly activities are similar whether dealing with a single large die or multiple smaller die, with some of the main cost drivers being driven by area rather than number of chips

Initial Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.93
Total	**1.00**	**1.04**	**0.93**	**1.04**

All cost categories shown relative to the Monolithic Die scenario, except Interposer/Fan-out module, which is shown relative to the Silicon Interposer case

- Interposer/Fan-out Module
  - Cost only exists for the advanced packaging scenarios
  - Creating a silicon interposer for this application is more expensive than either of the fan-out scenarios
  - Creating a fan-out module for placement on a substrate is the least expensive option, since there are no topside RDLs or large copper pillars
  - Creating a fan-out module with embedded bridges and a topside RDL is slightly less expensive than creating an interposer

Initial Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.93
Total	**1.00**	**1.04**	**0.93**	**1.04**

All cost categories shown relative to the Monolithic Die scenario, except Interposer/Fan-out module, which is shown relative to the Silicon Interposer case

- Can the chiplet scenarios become more cost-effective?

Adjusted Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.93
Total	**1.00**	**1.04**	**0.93**	**1.04**

- Assume a 35x35mm substrate for all advanced packaging scenarios, instead of 40x40
- Assume the interposer and fan-out module size only needs to be 25x25mm, instead of 30x30

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.04	1.04	1.04
Die	1.00	0.61	0.61	0.61
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.91
Total	**1.00**	**0.94**	**0.85**	**0.94**

Adjusted Results: 10nm

	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.31	1.31	1.31
Die	1.00	0.61	0.61	0.64
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.93
Total	**1.00**	**1.04**	**0.93**	**1.04**

- Assume a 35x35mm substrate for all advanced packaging scenarios, instead of 40x40
- Assume the interposer and fan-out module size only needs to be 25x25mm, instead of 30x30

All chiplet scenarios are now cost-effective

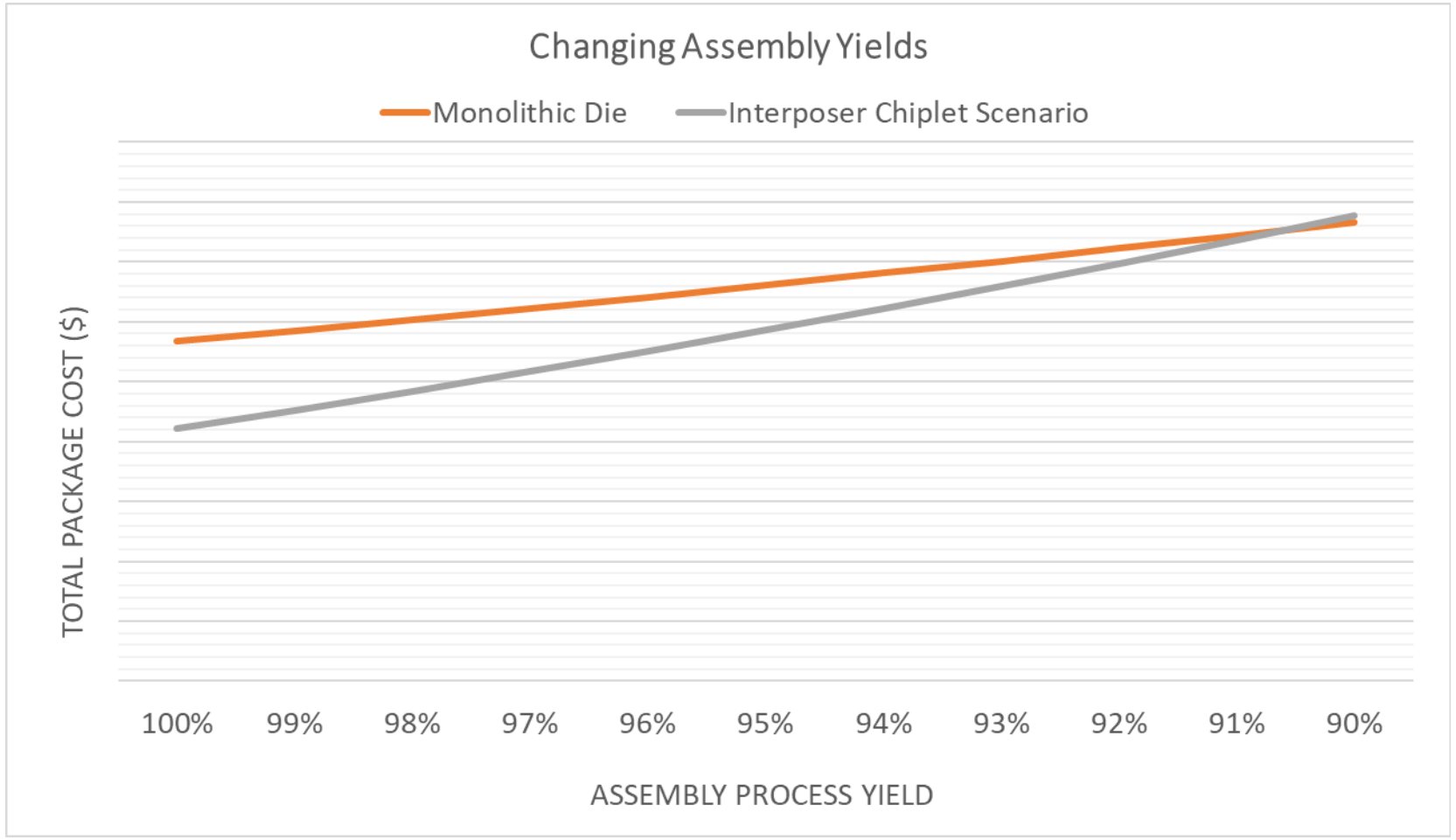
	Monolithic Die	Silicon Interposer	Fan-out on Substrate	Embedded Silicon Bridges
Substrate	1.00	1.04	1.04	1.04
Die	1.00	0.61	0.61	0.61
Die Prep	1.00	0.94	0.94	0.94
Assembly to Substrate	1.00	1.01	0.99	1.01
Interposer/Fan-out Module	0.00	1.00	0.65	0.91
Total	**1.00**	**0.94**	**0.85**	**0.94**

Yield

- Monolithic die with flip chip packaging
  - Assuming known good die AND known good substrate, 1 yield loss point to consider during packaging
    - Assembling the good die to the good substrate
- Interposer-based chiplet packaging
  - Assuming known good chiplets AND known good substrate, 3 yield loss points to consider during packaging
    - Interposer creation – The interposer will have some defects prior to any chiplets being bonded
    - Assembly of chiplets to interposer
    - Assembly of chiplet+interposer stack to substrate
- Next chart changes the assembly yields
  - Use final version of design examined:

Die and Chiplet Details	Interposer Scenario	Monolithic Die	Silicon Interposer
20x20mm 10nm die (on a 30x30mm substrate) vs. 4 chiplets: 10nm, 45nm, 28nm x2	25x25mm interposer, 35x35mm substrate	1.00	0.94

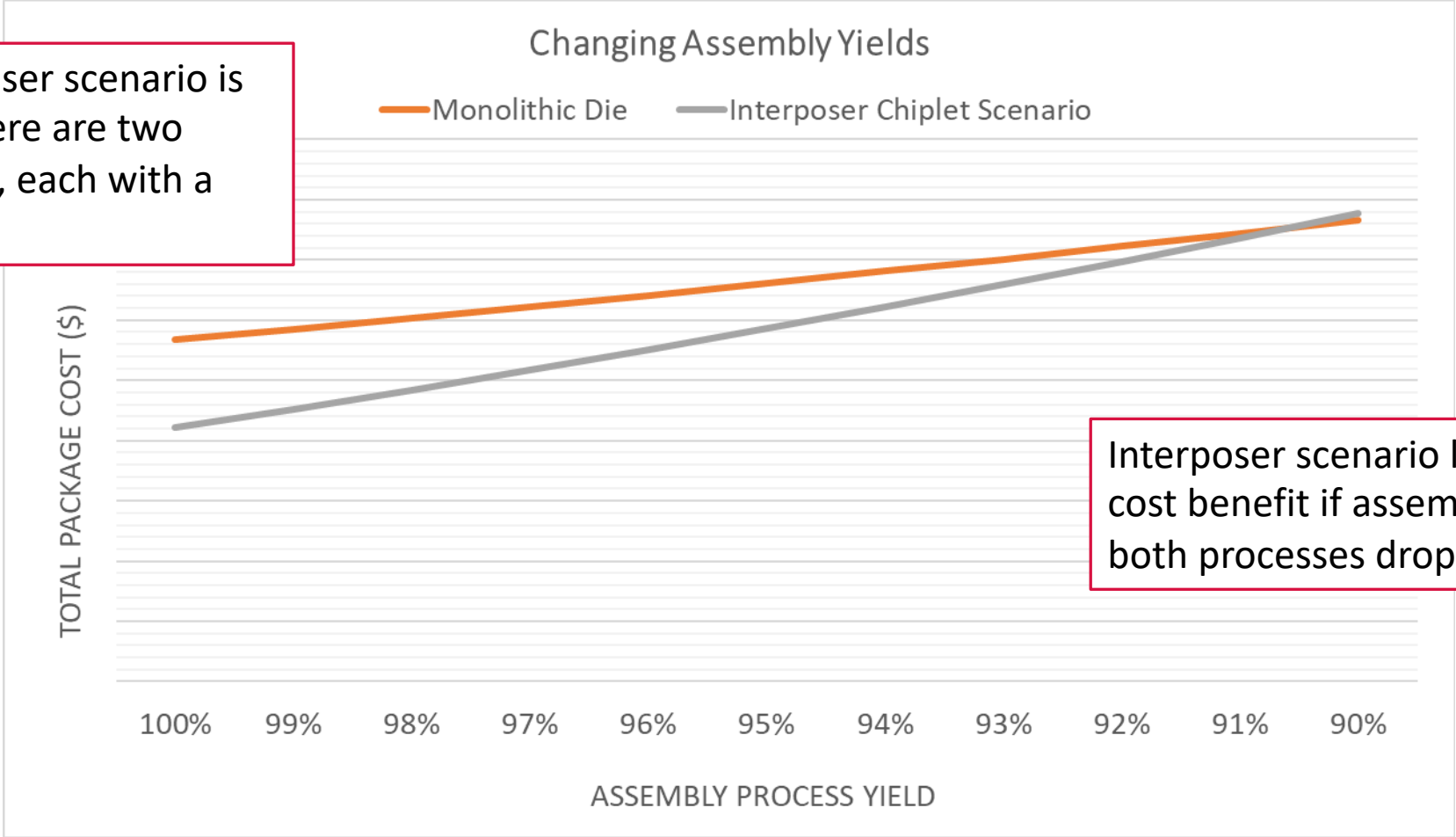
Changing Assembly Yields



Design: One 10nm die versus 4 chiplets at 10nm, 45nm, 28nm x2 | FC substrate: 30x30mm | Interposer substrate: 35x35mm | Interposer size: 25x25mm

Changing Assembly Yields

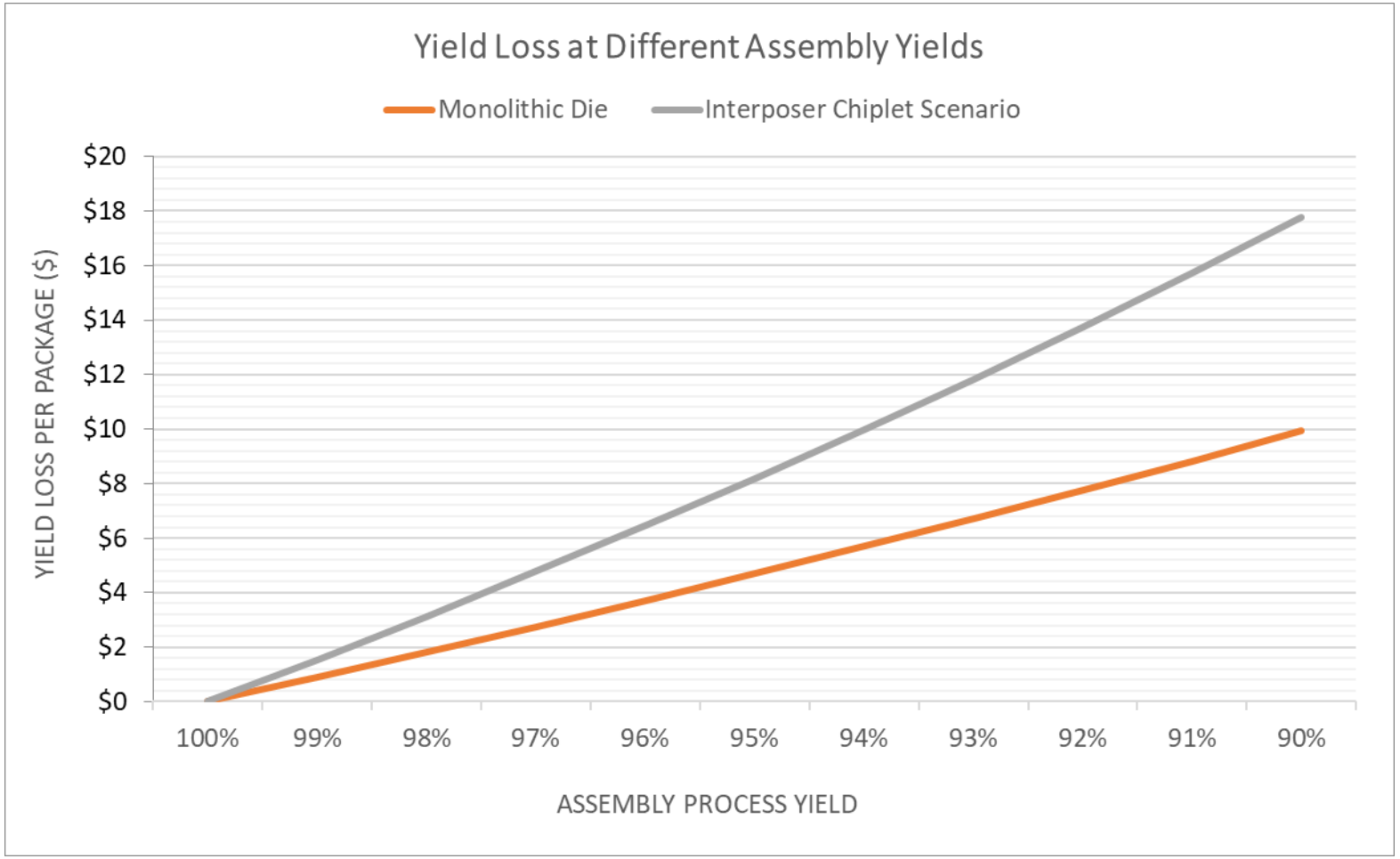
Slope of the interposer scenario is steeper because there are two assembly processes, each with a yield hit



Interposer scenario loses its small cost benefit if assembly yield for both processes drops too much

Design: One 10nm die versus 4 chiplets at 10nm, 45nm, 28nm x2 | FC substrate: 30x30mm | Interposer substrate: 35x35mm | Interposer size: 25x25mm

Changing Assembly Yields



Design: One 10nm die versus 4 chiplets at 10nm, 45nm, 28nm x2 | FC substrate: 30x30mm | Interposer substrate: 35x35mm | Interposer size: 25x25mm

Additional Yield Considerations

- Previous charts focused on the impact of assembly yields only
  - Simple trade-off
- Yield of interposer or fan-out creation process is another factor
- Yield of incoming die will factor into the real world
  - Trade-off between a higher price for known good die or yield risk with not-known good die
- Yield of incoming substrate will be another factor

Summary

- Basic tradeoff between a monolithic die and a series of chiplets is a **reduction** in die costs countered by an **increase** in packaging costs
- Various advanced packaging technologies are emerging to support chiplets
  - Chiplet on interposer on substrate, fan-out on substrate, and fan-out with embedded silicon presented
  - Fan-out on substrate is the simplest of the three
  - Interposer-based process and fan-out with embedded silicon had similar costs in the design analyzed
  - Chiplet size, chiplet nodes, required package size, required substrate size, and number of RDLs are some of the design attributes that will determine whether chiplets are cost-effective
- Yield is complicated
  - Must consider the yield of: the substrate, incoming die/chiplets, fan-out or interposer creation process, chiplet assembly, and assembly-to-substrate process
  - Simple assembly yield analysis showed that scrap costs are higher for chiplet scenarios at the same assembly yield as a monolithic die solution

Thank you!

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