

Electronics test and production improvements from algorithmic methods to unsupervised machine learning

Ron Press, Sr. Director, Technology Enablement, Tessent, June 2024

Why AI for EDA and test?

AI is exciting and changing everyday life

AI isn't a replacement for engineering innovation

Electronics Design Automation (EDA) automates processes as they get more complicated

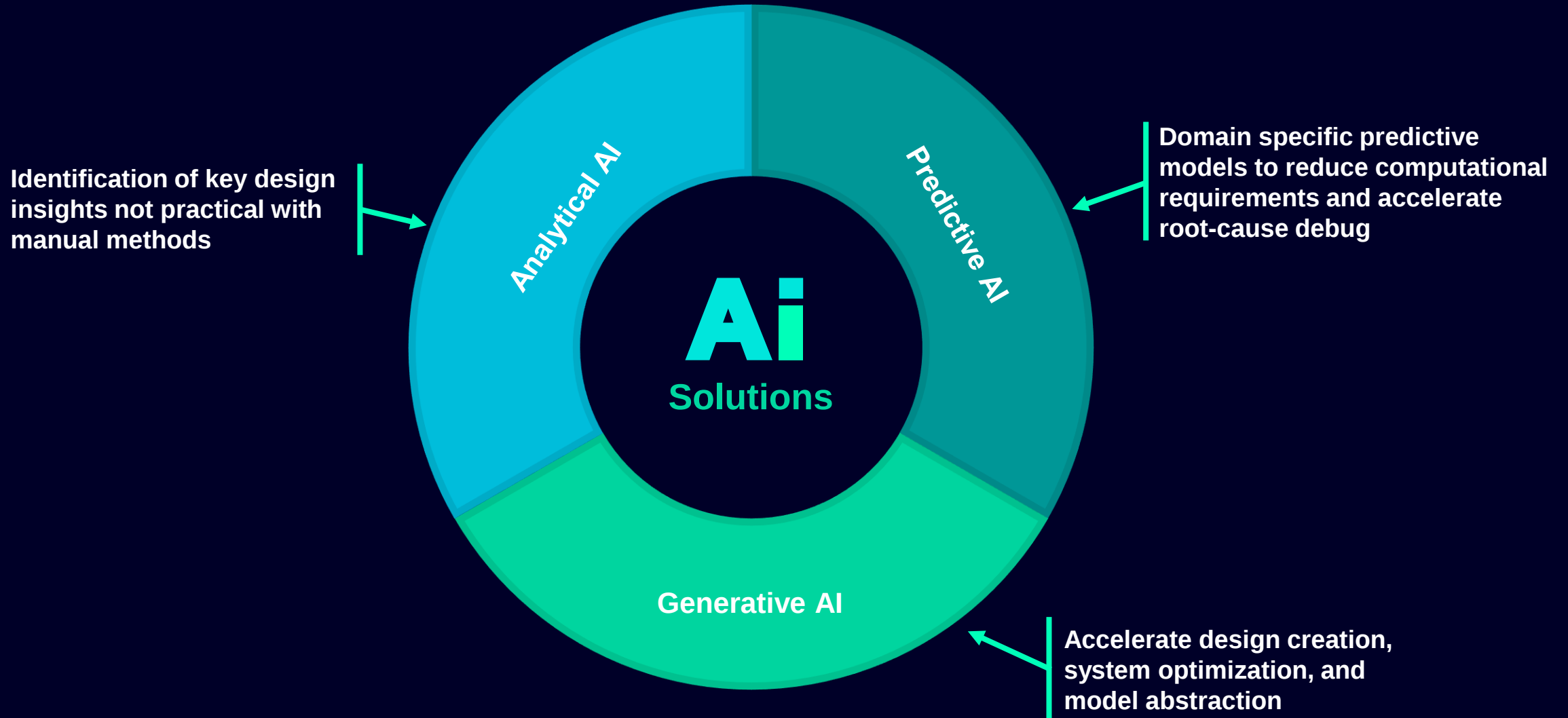
- Users can work at a higher level of automation/abstraction
- A significant amount of work is rules checking to verify results

DFT workflows

- DFT architecture and ATPG – affects design and test engineering
- Scan diagnosis and yield learning – takes the production fail results to improve yield

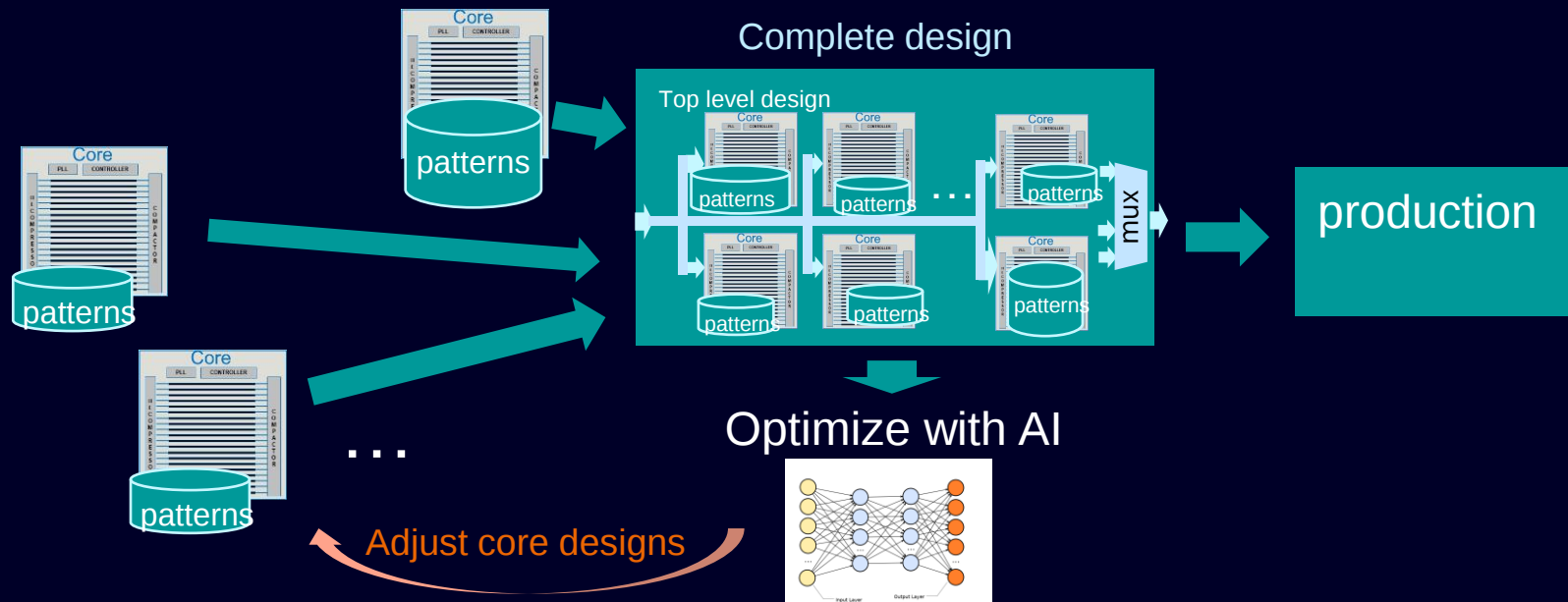


AI spans modeling technologies to deliver productivity



Applying AI to optimize DFT

Core designs optimized with other cores to balance chip IO bandwidth allocation
Lots of variables to balance



Traditional architecture:

- Not flexible or resilient (core ECOs)
- Static and can't change
- Stuck if top level design is frozen
- Requires all core DFT and patterns ready
 - Late in design flow

New packetized test solution using Analytical AI

Tessent SSN is a new approach for production test, is a form of Analytical AI or “adaptive intelligence”

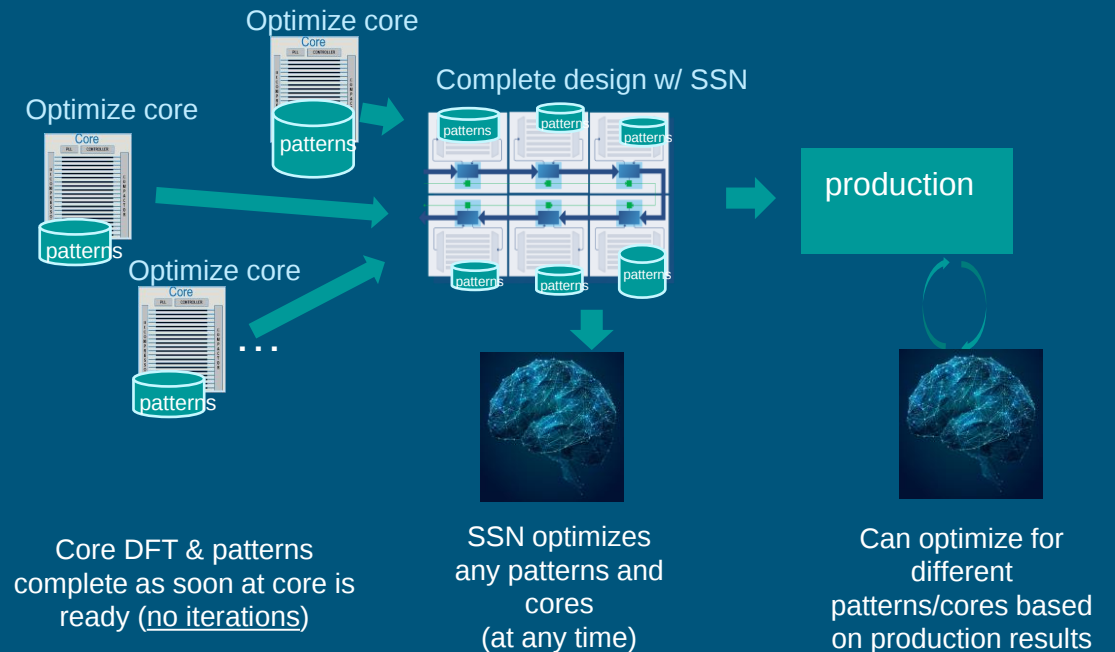
- Removes dependency between core test IO/patterns and top-level IO
- Provides flexibility via s/w algorithms to test any set of cores and patterns
- s/w automatically performs optimizations

10x productivity improvement

Up to 5x test time improvement

6x test power reduction

SSN removes DFT architecture variables and automatically optimizes test solution at any time

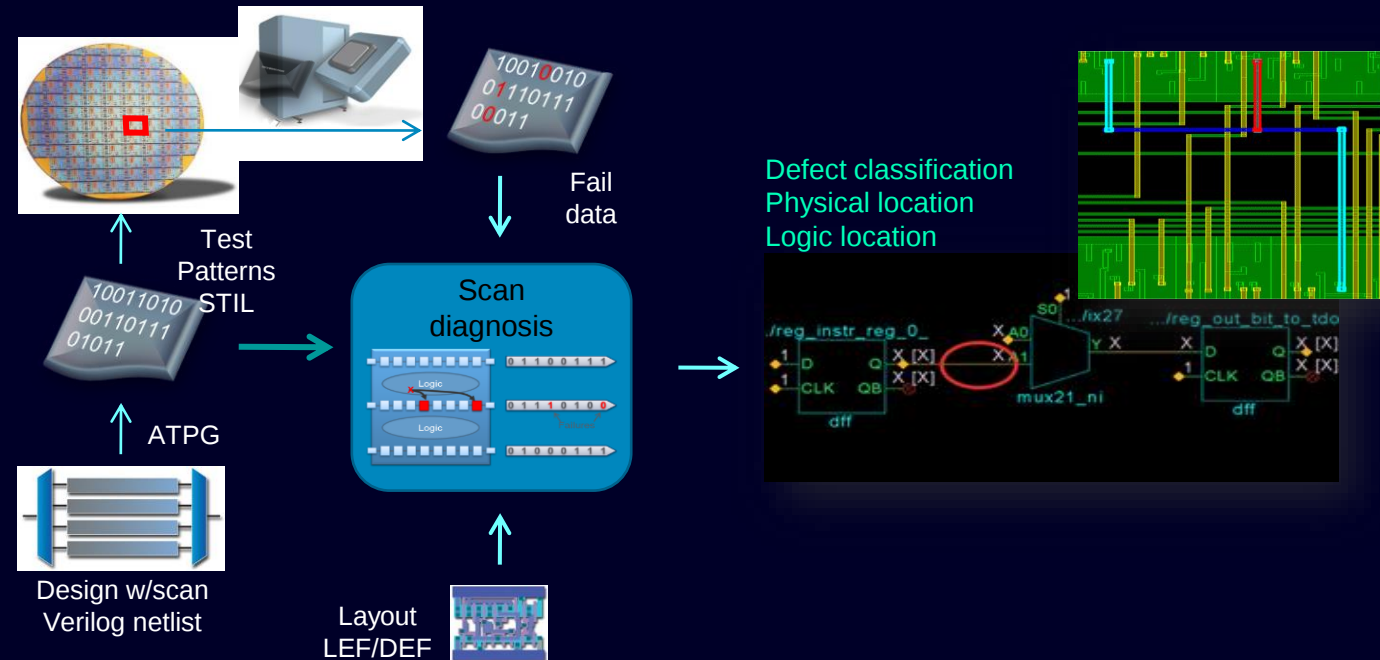


Scan diagnosis provides a digital twin for failure analysis (FA)

Scan test provides millions of virtual sample sites during production test

Scan diagnosis pinpoints failing test locations very quickly

Scan diagnosis enables quick callouts of 1000s, 10s of thousands or more failure locations for big data analysis with ML

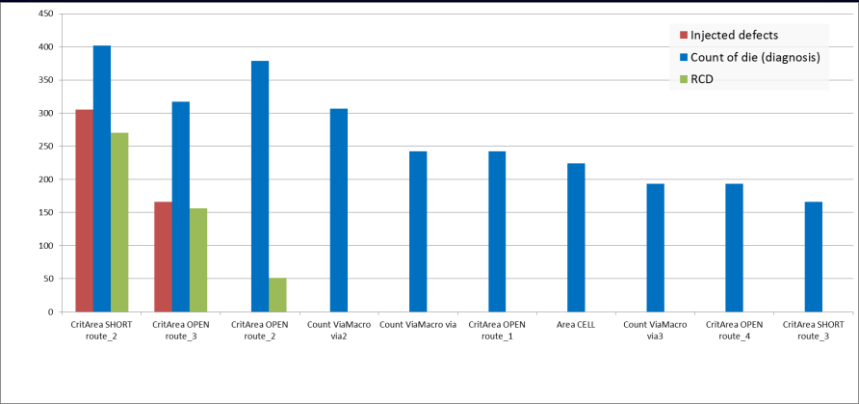


AI enabled yield improvement based on production scan test failures

	RCD - Sum of Probability	Total	CRF	Pareto
0	CritArea SHORT route_2	269.963	0.565	
1	CritArea OPEN route_3	156.503	0.892	
2	CritArea OPEN route_2	51.534	1.000	

DieID	X	Y	CritArea SHORT route_2
1464	18	38	0.997
244	46	28	0.996
731	11	36	
1387	28	21	
969	29	9	

suspect	score	fail_match	pass_mismatch	type	value	pin_pathname	cell_name	net_pathname	layout_status	
1	100	30	0	BRIDGE_2WAY	0	/cpu_i/ix1226/Y buf02	/cpu_i/ix1227	LOCATION_IN_LAYOUT		
suspect	score	fail_match	pass_mismatch	type	value	pin_pathname	cell_name	net_pathname	layout_layer	critical_area
1.1	100	30	0	BRIDGE_2WAY	0	/cpu_i/ix1222/Y buf02	/cpu_i/ix1222	route_1	route_1	8.94E+01
								route_2	route_2	3.34E+02
								route_3	route_3	1.45E+00
								route_4	route_4	1.12E+02
								route_5	route_5	6.83E+00



Tessent YieldInsight has been employing and refining unsupervised machine learning for over a decade

- Over three million production fail diagnoses performed every day
- ML automation finds systematic yield limiters

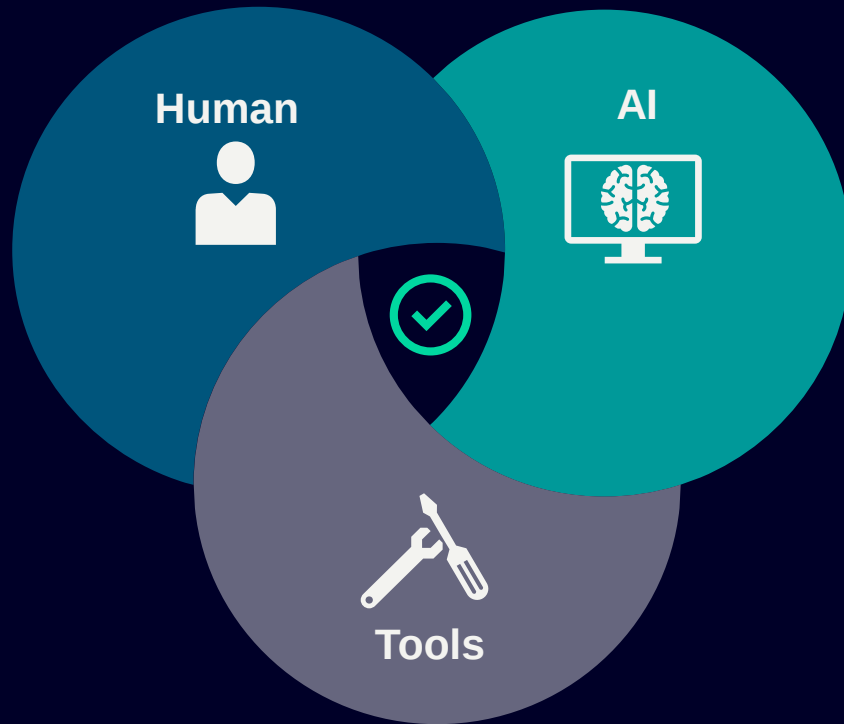
2x improvements in diagnosis accuracy and resolution

2.5% improvement in yield above entitlement

Tessent AI capabilities and industry impact

Company	Benefit	Reference	Technology
UMC	11x diagnosis resolution improvement w/ RCAD	International Test Conf 2020 paper	Unsupervised ML
Qualcomm	2-4x physical failure analysis improvement	ISTFA 2021 paper	Unsupervised ML
Qualcomm	4x chain diagnosis resolution	International Test Conf 2022	Unsupervised ML
Intel	10x productivity improvement for DFT architecture	International Test Conf 2020	SSN adaptive intelligence
Amazon	5x production test time improvement	International Test Conf 2022 video	SSN adaptive intelligence

Verifiable AI closes the loop to deliver trusted results



The **synergy** of human insights, AI and foundation tools delivers **Verifiable AI** to meet the challenges of the next frontier for semiconductor development

Thank you

Questions?



References

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 - **Using Volume Cell-aware Diagnosis Results to Improve Physical Failure Analysis Efficiency**
- Qcomm 2-4x – <https://ieeexplore.ieee.org/document/9983907>
 - S. Mittal et al., "Industry Evaluation of Reversible Scan Chain Diagnosis," 2022 IEEE International Test Conference (ITC), Anaheim, CA, USA, 2022, pp. 420-426,
 - Additional - <https://dl.asminternational.org/istfa/proceedings-abstract/ISTFA2021/84215/388/18305>
 - **Improving Diagnosis Resolution with Population Level Statistical Diagnosis - webinar**
- Qcomm 4x chain – <https://register.gotowebinar.com/register/902956749512083214?source=Website>
 - [Novel Reversible Scan Chain Technology that Improves Chain Diagnosis Resolution by 4X](#)
- Intel – <https://ieeexplore.ieee.org/document/9325233>
 - **Streaming Scan Network (SSN): An Efficient Packetized Data Network for Testing of Complex SoCs**
- Amazon – <https://resources.sw.siemens.com/en-US/video-dan-trock-amazon-how-aws-benefited-from-tessent-ssn>
 - <https://www.youtube.com/watch?v=CYPqna1ac-4>
 - **How Amazon Web Services reduced design effort, test time & power using Tessent SSN**

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**THE APPLICATION OF NEURAL NETWORK TECHNOLOGY TO
BUILT-IN TEST FALSE ALARM FILTERING**

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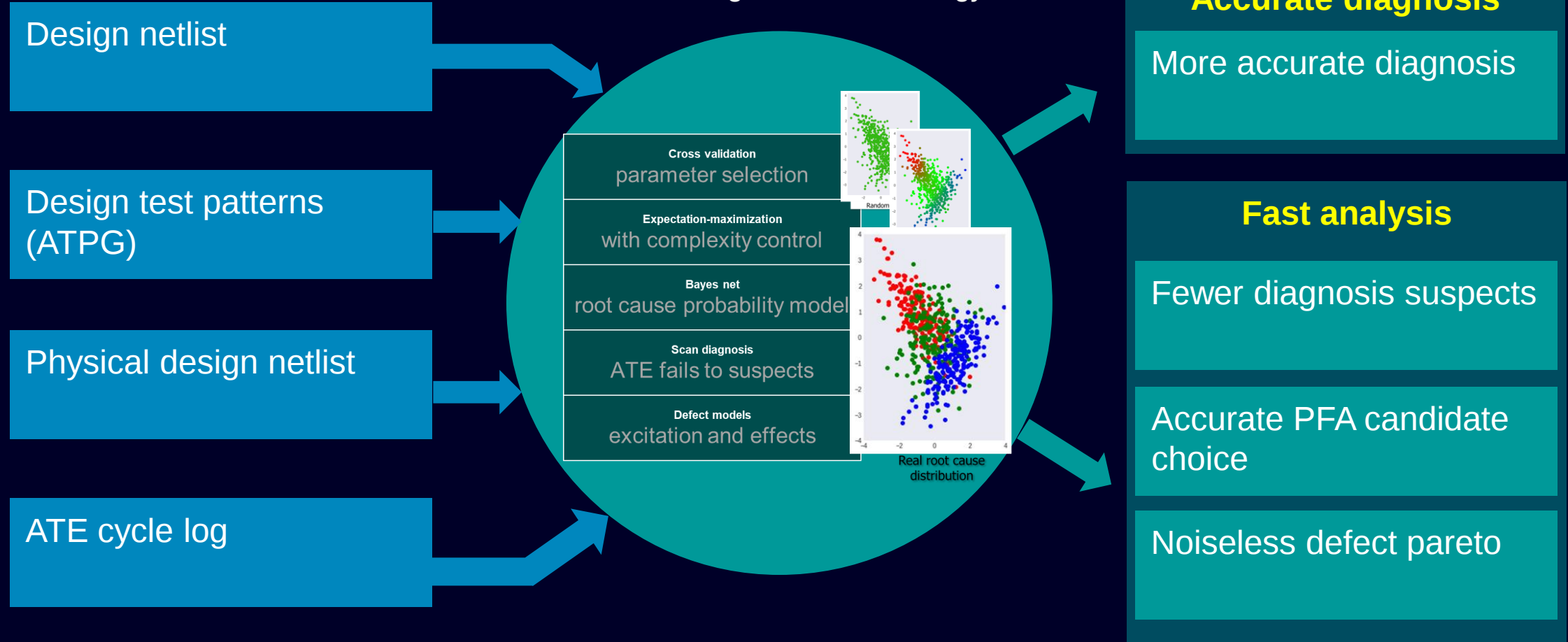
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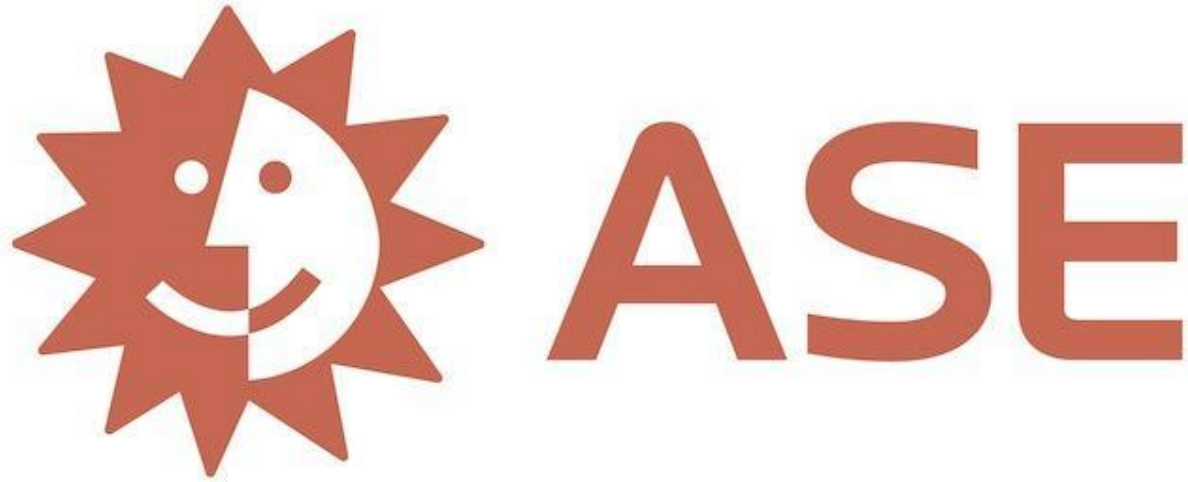
Applying ML for impactful diagnosis on yield analysis

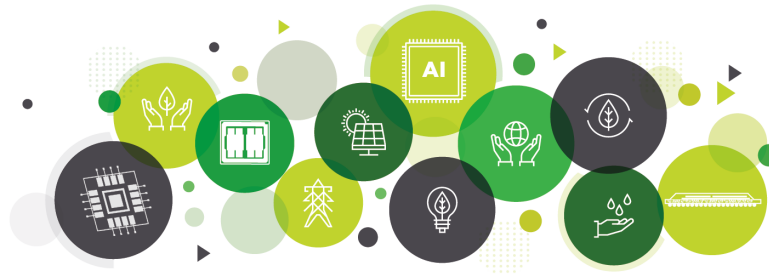
Diagnosis Driven Yield Analysis

Machine Learning based technology stack



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