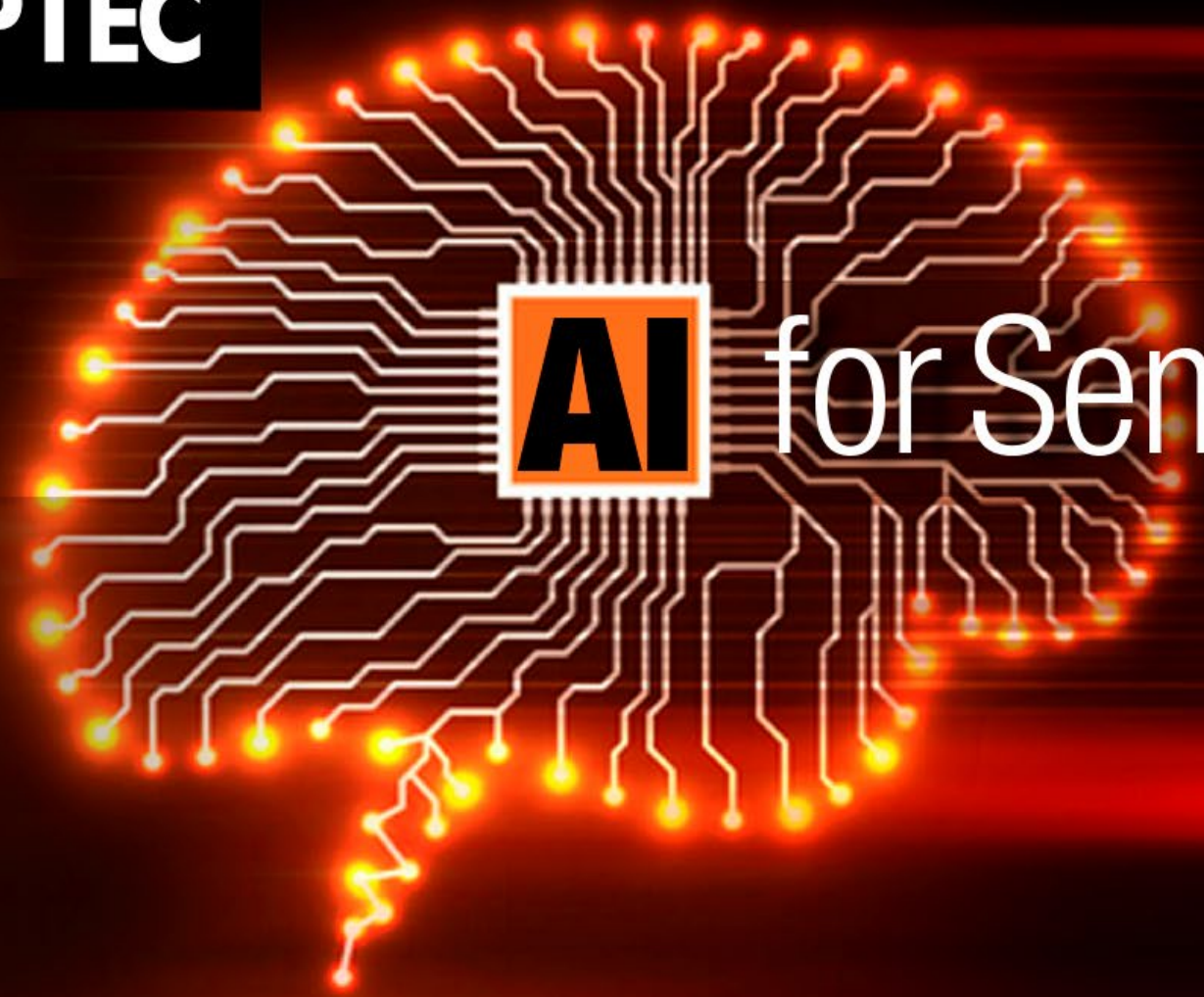
MEPTEC



AI for Semiconductors

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Accelerating PCB Design With AI

June 2024

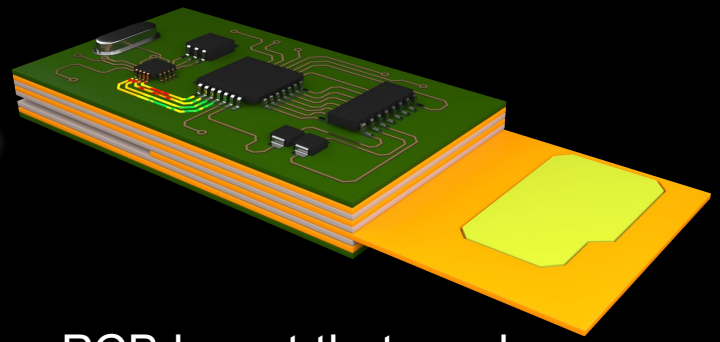
Taylor Hogan
Distinguished Engineer

cadence®

Allegro X AI Inputs and Outputs

Brings automation approach of IC digital design to PCB

Design Netlist
and
Constraints



PCB layout that can be used as generated or incrementally modified

AI In X AI

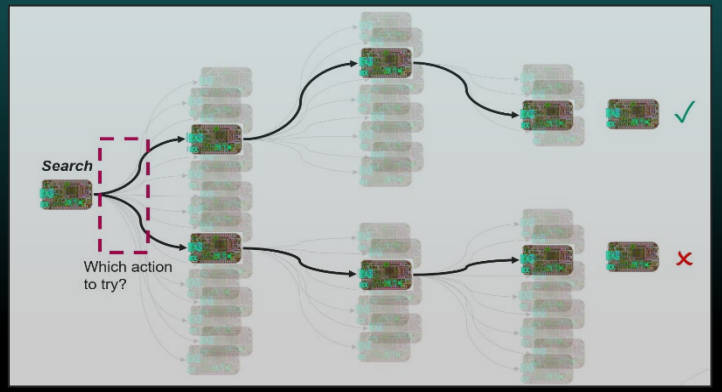
- Genetic Optimization
  - Chromosome contains “learned” good placement strategies
- Bayesian Optimization
  - Find the optimum set of hyper parameters used to guide automation
- Spectral Clustering
  - All AI Books contain k-means and other clustering techniques
- Monte Carlo Tree Search
  - Ala Alpha Go
- **Convolution Neural Net as a Proxy for a Router**
  - **Infers the probability of routing success given a placement**

Allegro X AI Placement Technologies Under the Covers

Extensive collection of AI and non-AI technologies powers X AI

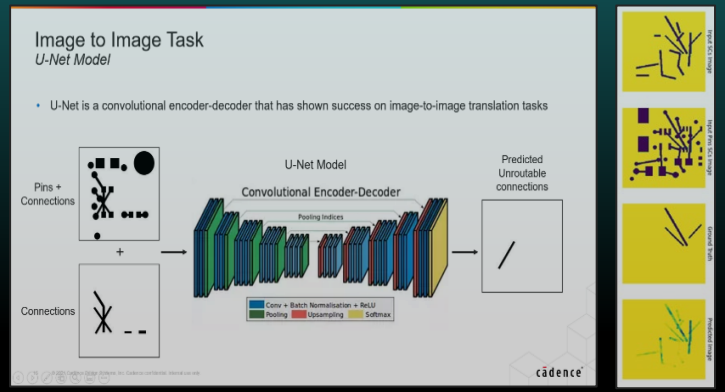
Monte Carlo Tree Search

Cloud Compute to Learn How to Incrementally Improve a Design



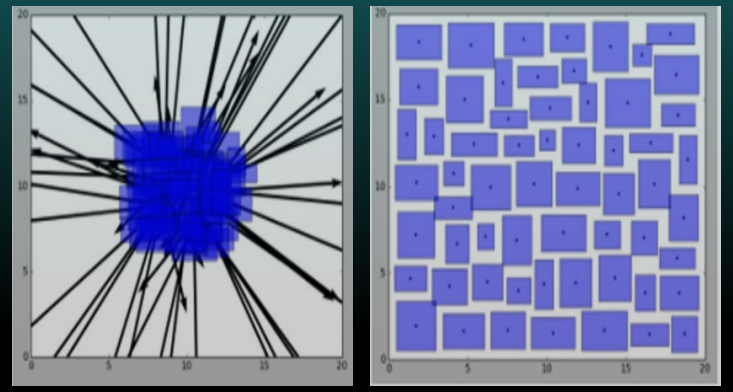
Convolutional Neural Net (CNN)

Predicts Routability to Guide Placement Refinement



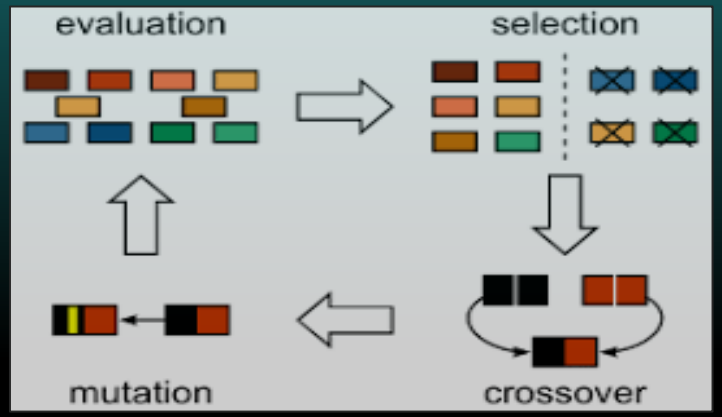
Force Directed Placement

Globally Optimizes Component Placement



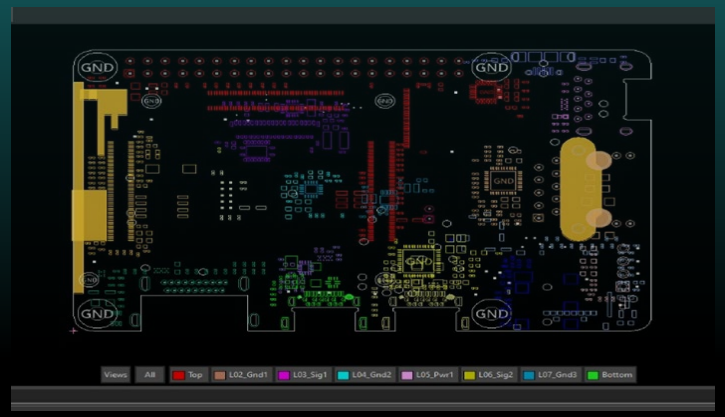
Distributed Genetic Optimization

Optimize Component Orientation/Rotation



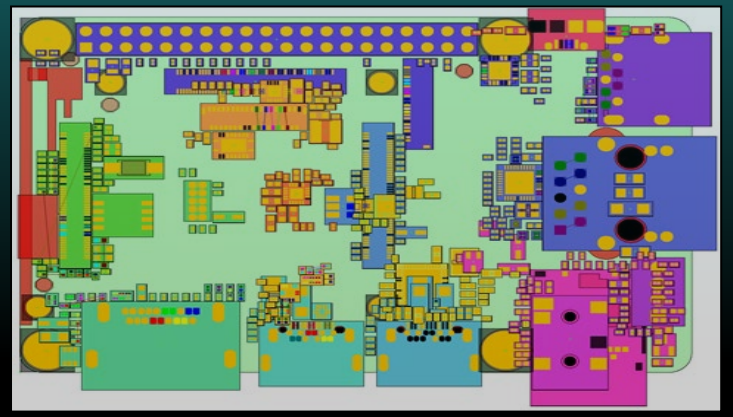
Spectral Clustering

Identifies Component Groupings

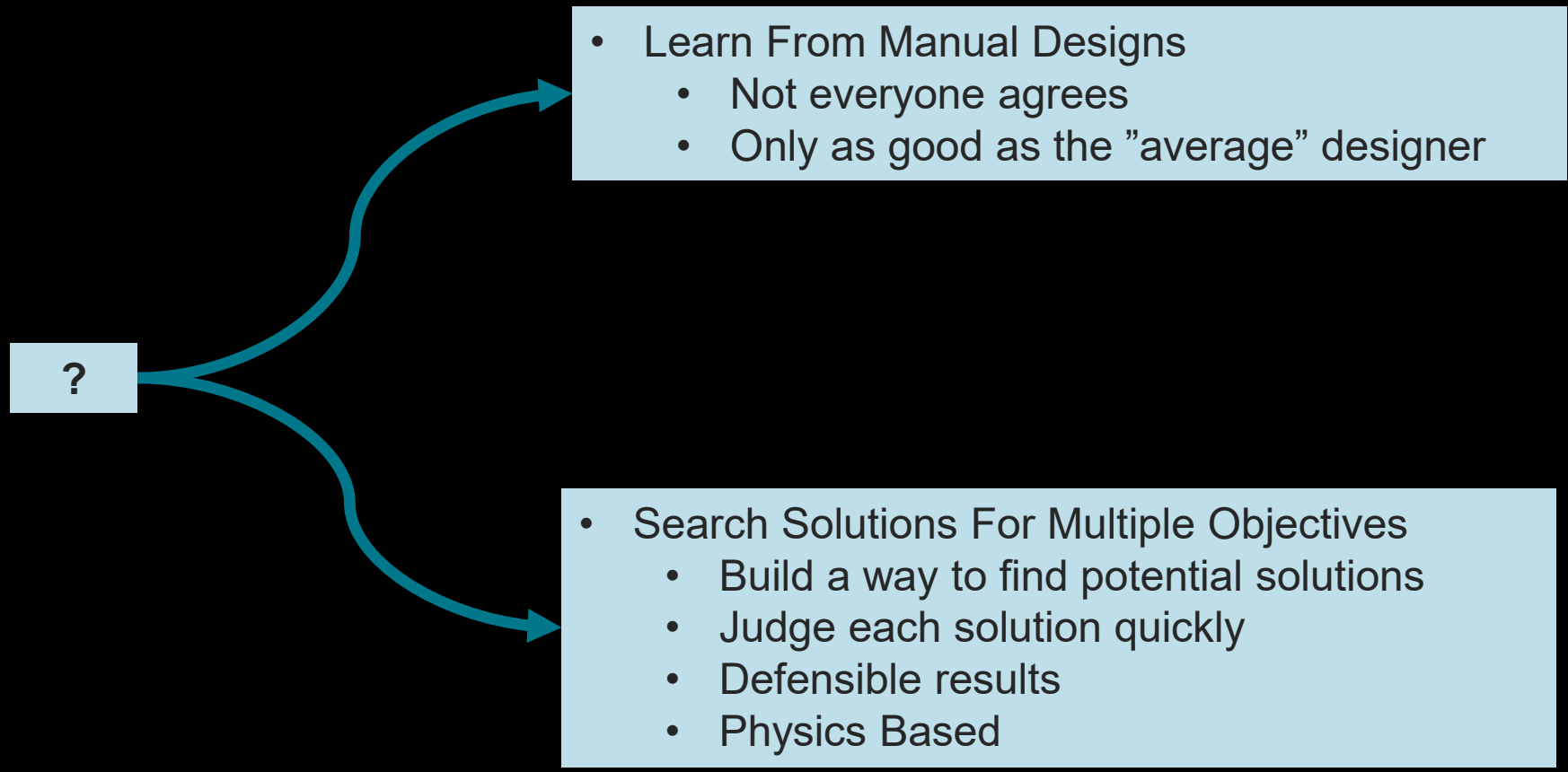


Route Aware Detailed Placement

Placement Legalization and Aesthetics



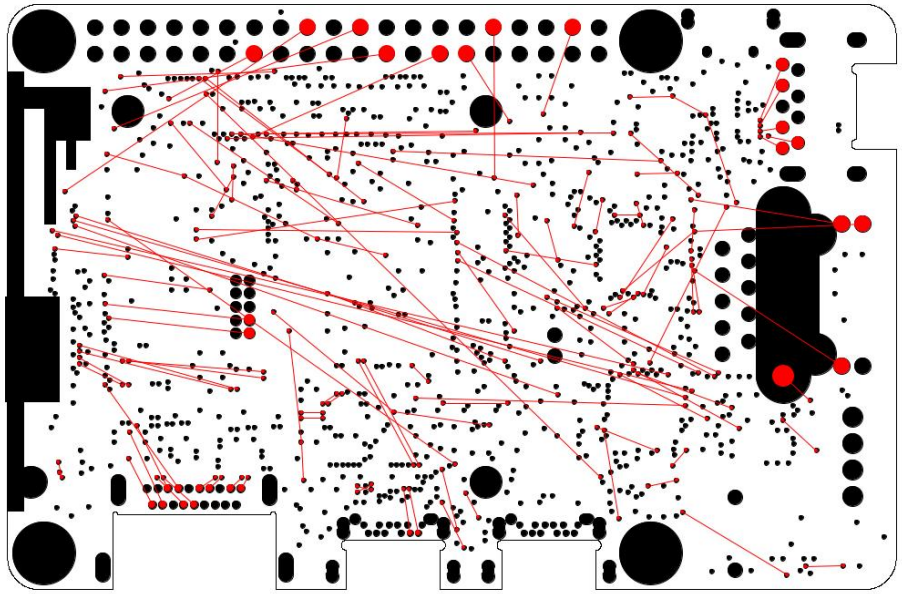
Automatic PCB Design…Which Strategy?



Route Prediction Problems

Can we predict the disconnects before we route?

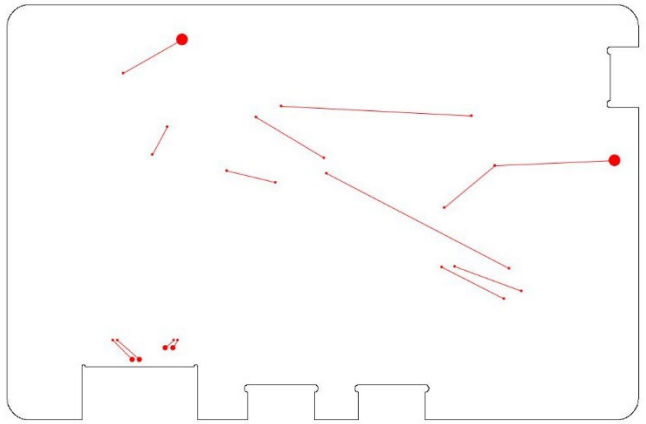
Connections



Model

Score: 97% Complete

Scores/Predictions

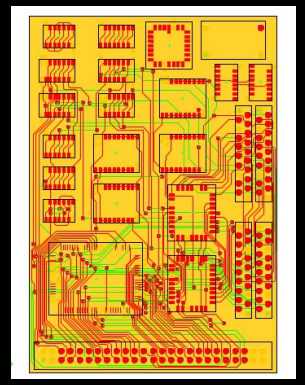


Route Prediction Problems

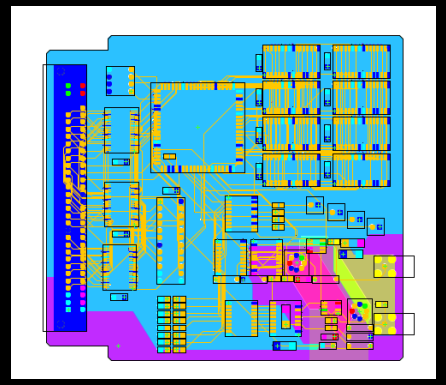
Building a Dataset

	Board 1	Board 2	Board 3	Board 4	Board 5	Board 6
Training Set Size	12,136	12,362	12,320	20,878	12,761	
Test Set Size	2,962	4,038	4,168	3,102	3,260	1,663

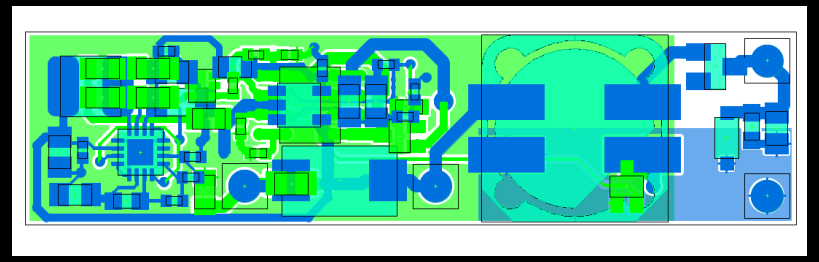
Simple

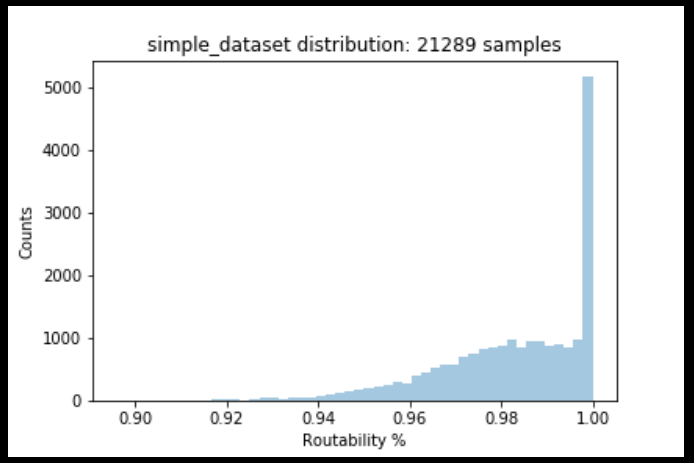


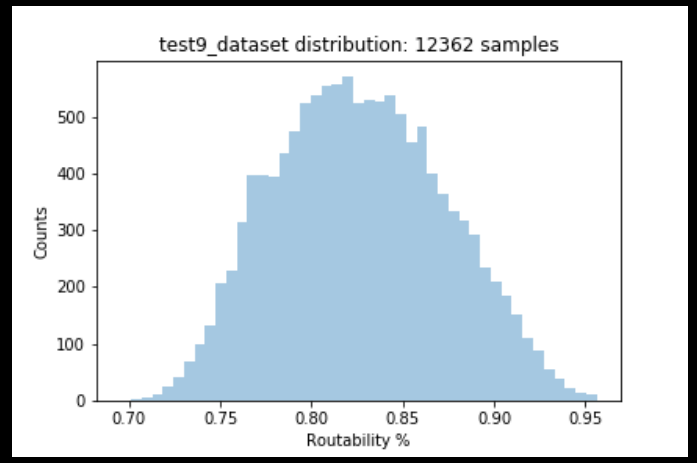
Test9

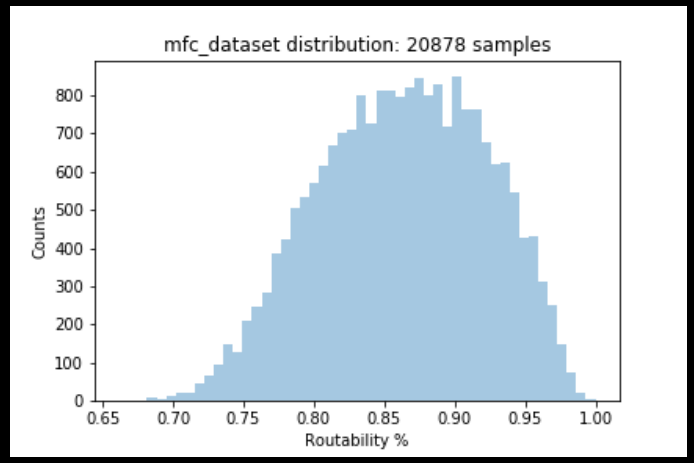


MFC_TI_Flyback_Rev2





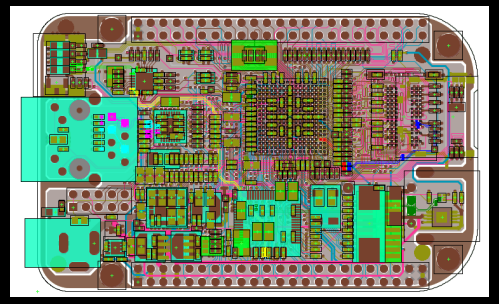




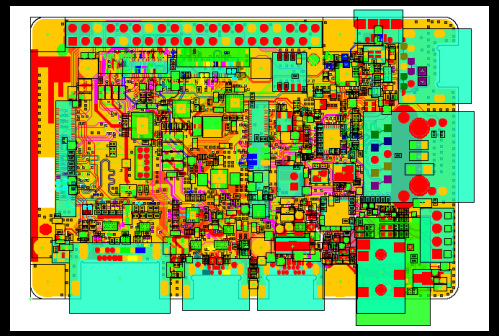
Route Prediction Problems

Quick turn around and Automatic Labeling

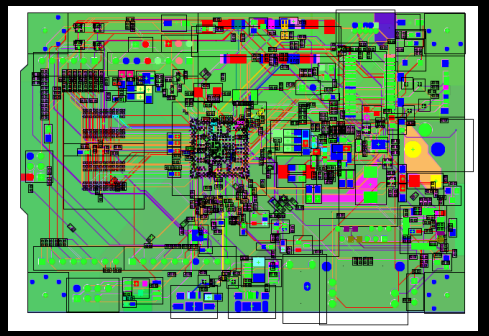
BeagleBone

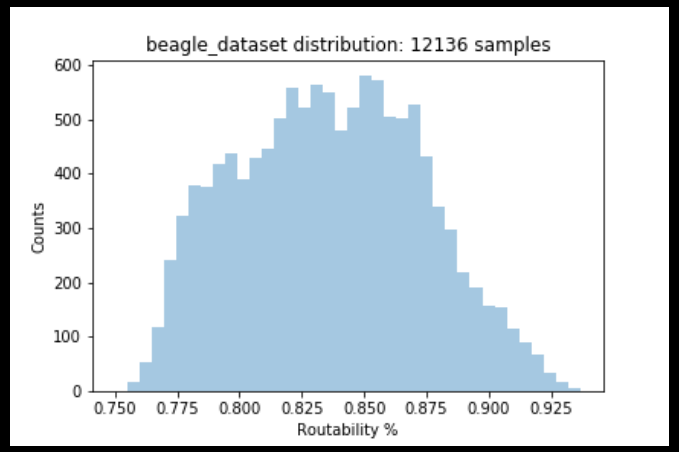


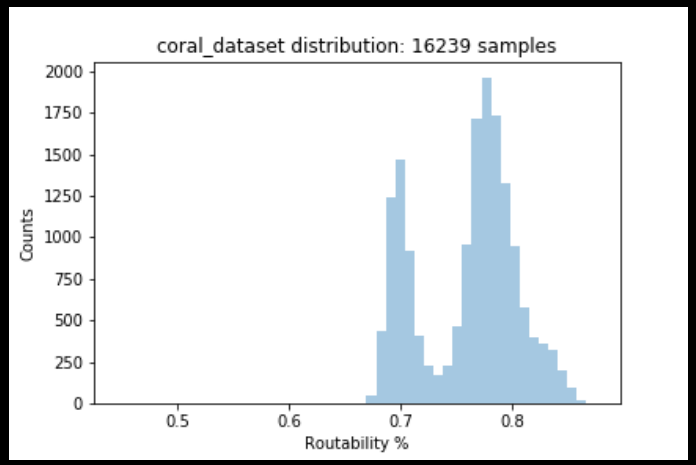
Coral

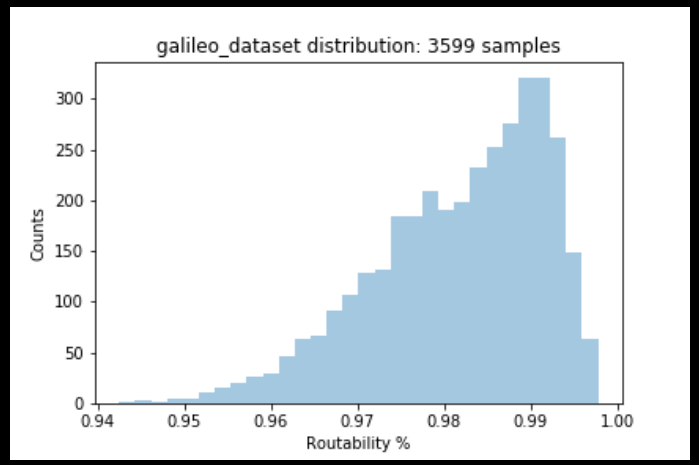


Galileo_G87173_204



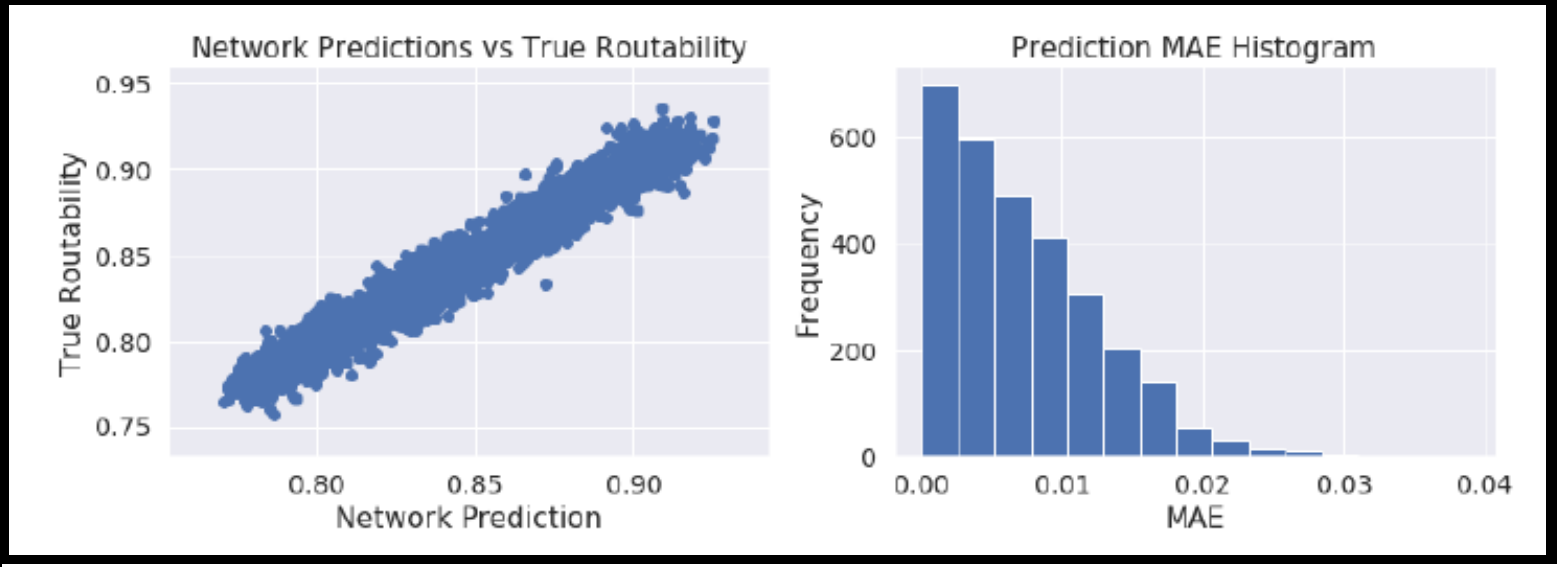


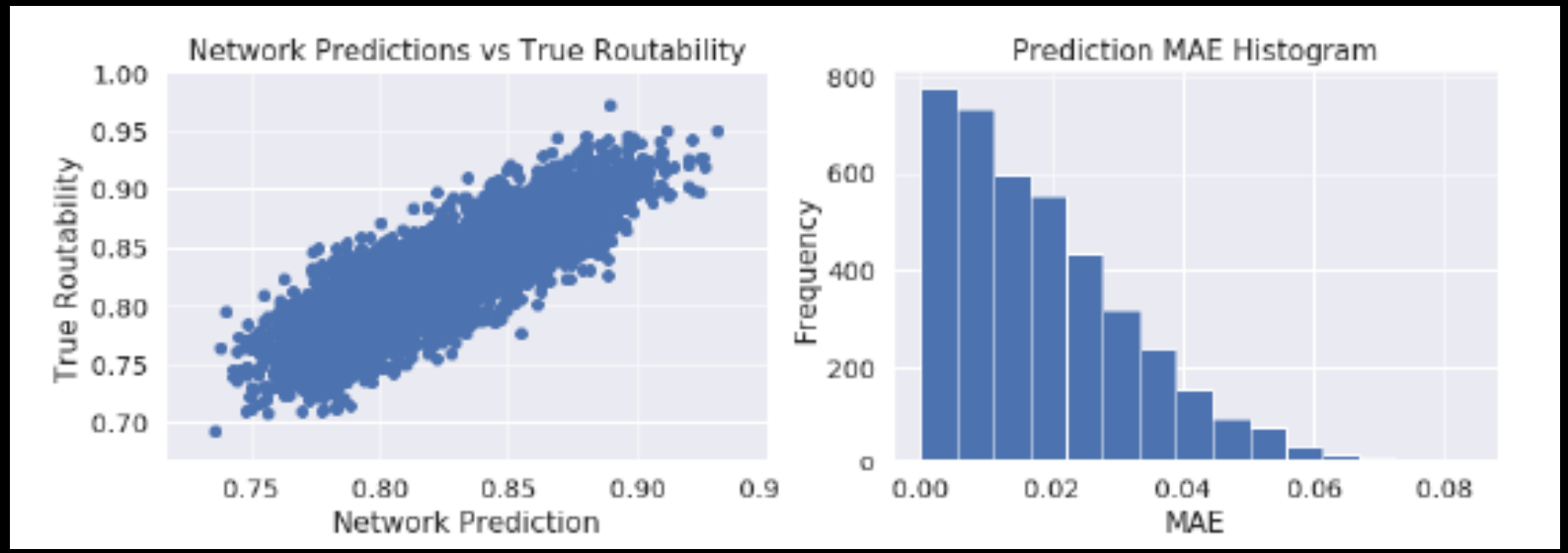




Learning to Score Designs

How do NNs correlate with Routability?



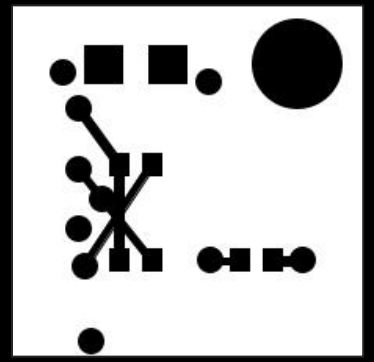


Disconnection Prediction Task – Via Patch Model

U-Net Model

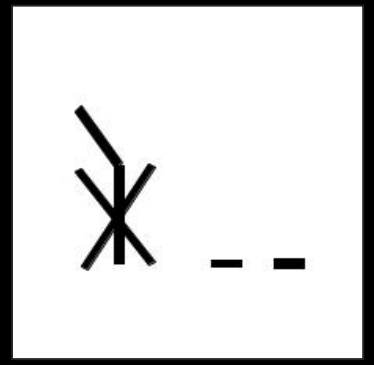
- U-Net is a convolutional encoder-decoder that has shown success on image-to-image translation tasks

Pins + Connections

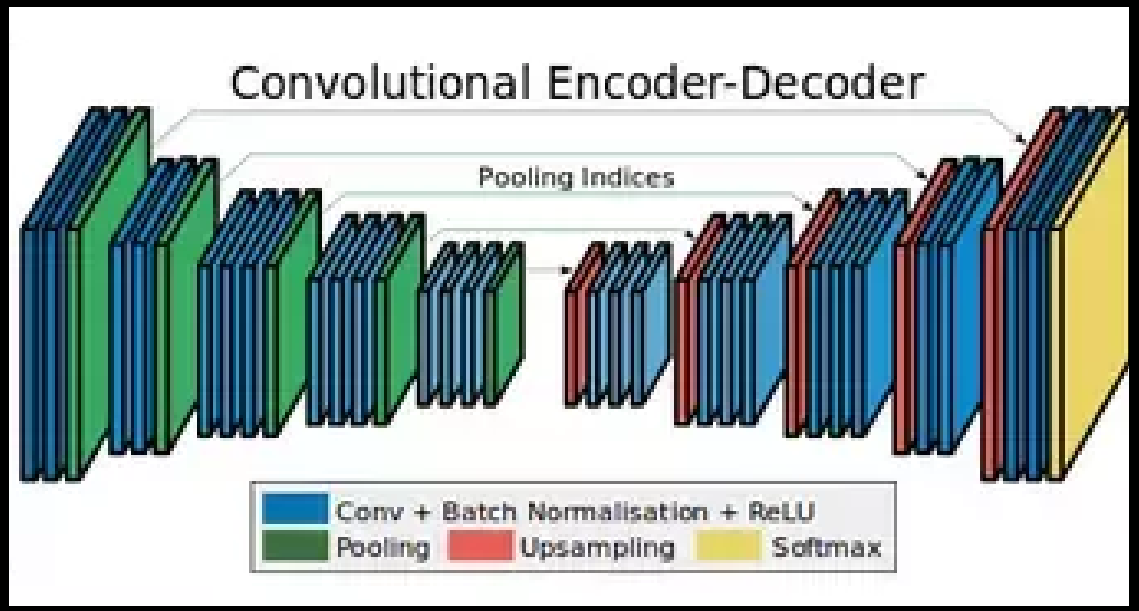


+

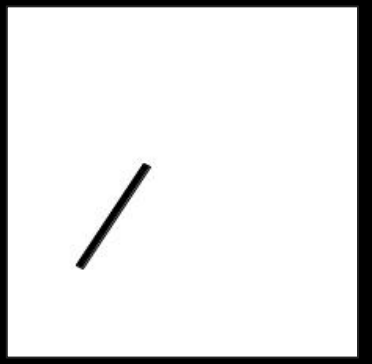
Connections



U-Net Model

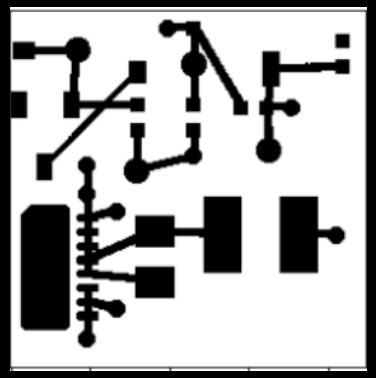


Predicted Unroutable connections

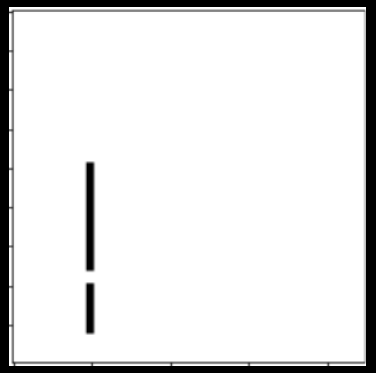


Disconnect Prediction Task

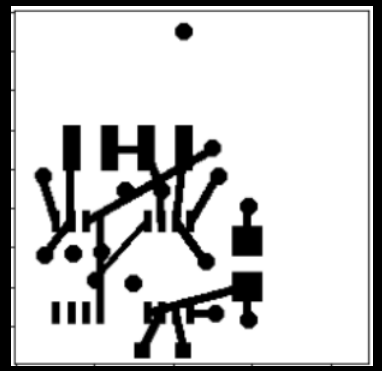
Input feature:

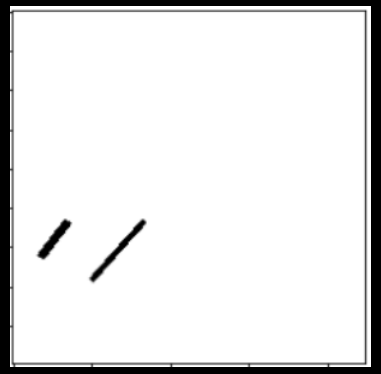


Label:



Prediction:



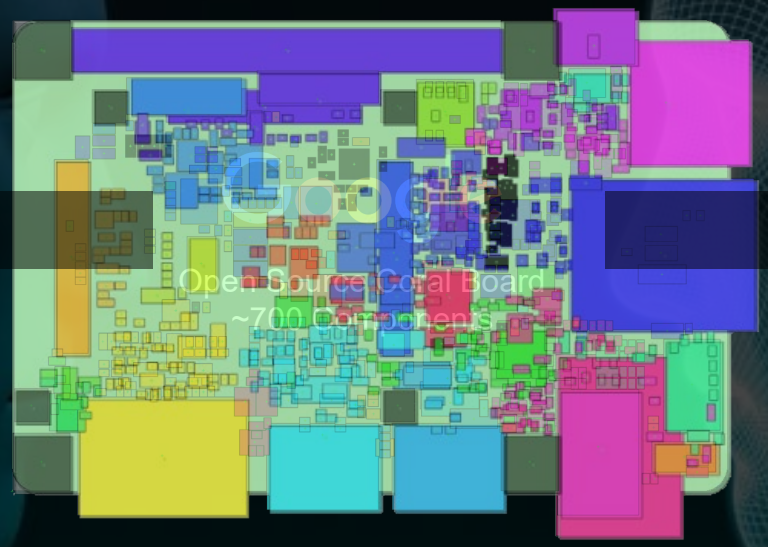


Allegro X AI Results

Transforming IC packaging and PCB

PLACEMENT	WIRELENGTH	MANUFACTURING	ELECTRICAL ANALYSIS
3 days to 75 Minutes	**12% Improved**	**100% Compliant**	**Optimized**

Human



X AI

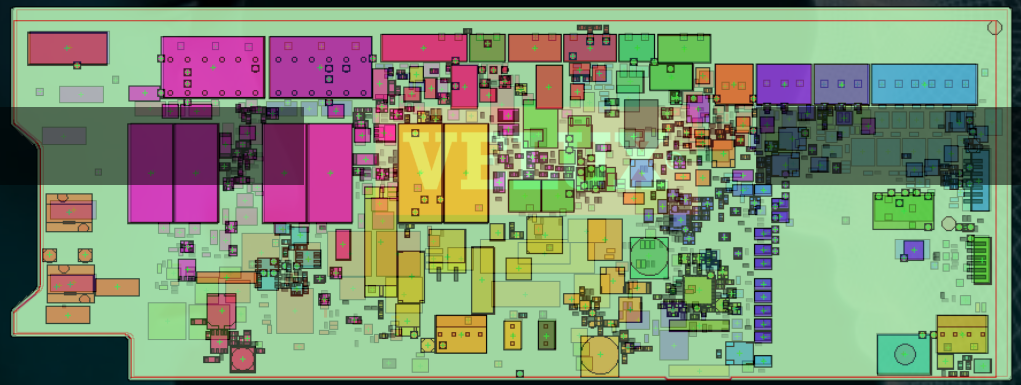
Leverages Cadence® OnCloud to evaluate 1000s of alternatives

Allegro X AI

Transforming IC packaging and PCB

PLACEMENT	WIRELENGTH	MANUFACTURING	ELECTRICAL ANALYSIS
4 days to 2 hours	1% Improved	100% Compliant	Optimized

Human



X AI

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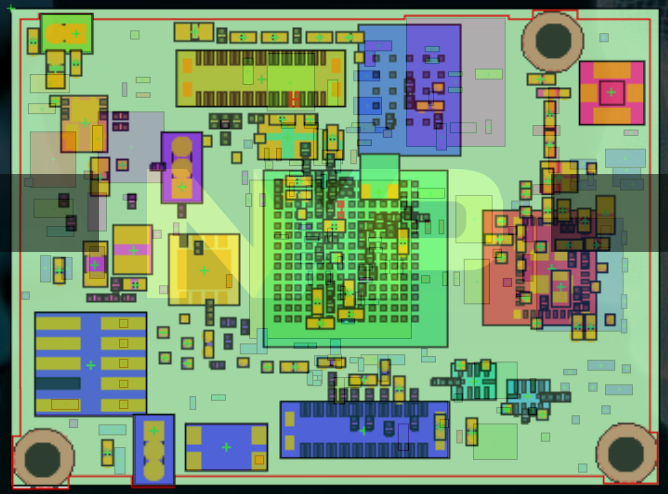
Allegro X AI

Transforming IC packaging and PCB

PLACEMENT	WIRELENGTH	MANUFACTURING	ELECTRICAL ANALYSIS
22 hours to 34 minutes	10% Improved	100% Compliant	Optimized

Human



X AI

Leverages Cadence® OnCloud to evaluate 1000s of alternatives

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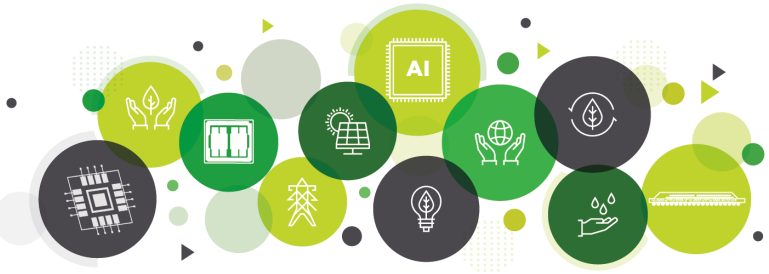

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